Datasheet

APM32F425xG_F427xG

Arm® Cortex® -M4F based 32-bit MCU

Version: V1.1

1 Product Characteristics

- **Core**
  - 32-bit Arm® Cortex®-M4F core with FPU
  - Up to 240MHz working frequency
- **Memory and interface**
  - Flash: The capacity is up to 1MB
  - SRAM: System (up to 448KB) + backup (4KB)
  - EMMC: Support CF card, SRAM, PSRAM, SDRAM, NOR and NAND memories
- **Clock**
  - HSECLK: 4~26MHz external crystal/ceramic oscillator supported
  - LSECLK: 32.768kHz crystal/ceramic oscillator supported
  - HSICLK: 16MHz RC oscillator calibrated by factory
  - LSICLK: 32kHz RC oscillator supported
  - PLL1: Phase locked loop; output frequency is configured by four parameters
- **Reset and power management**
  - V_{DD} range: 1.8~3.6V
  - V_{DDA} range: 1.8~3.6V
  - V_{BAT} range of backup domain power supply: 1.65V~3.6V
  - Power-on/power-down/brown-out reset (POR/PDR/BOR) supported
  - Programmable power supply voltage detector (PVD) supported
- **Low-power mode**
  - Sleep, stop and standby modes supported
- **DMA**
  - Two DMA; each DMA has 8 data streams, 16 in total
- **Debugging interface**
  - JTAG
  - SWD
- **I/O**
  - Up to 114 I/O
  - All I/O can be mapped to external interrupt vector
  - Up to 114 I/O pins tolerant to 5V input
- **Communication peripherals**
  - 4 USART, 2 UART, supporting ISO7816, LIN and IrDA functions
  - 3 I2C, supporting SMBus/PMBus
  - 3 SPI
  - 1 QSPI
  - 2 CAN
  - 2 USB_OTG controllers
  - 1 SDIO interface
  - 1 Ethernet
- **Analog peripherals**
  - 3 12-bit ADCs
  - 2 12-bit DACs
- **Timer**
  - 2 16-bit advanced timers TMR1/8 that can provide 7-channel PWM output, supporting deadband generation and braking input functions
  - 4 32-bit general-purpose timers TMR2/3/4/5, each with up to 4 independent channels to support input capture, output comparison, PWM, pulse count functions
  - 6 16-bit general-purpose timers TMR/9/10/11/12/13/14, each supporting input capture, output comparison, PWM, and pulse counting functions
  - 2 16-bit basic timers TMR6/7
  - 2 watchdog timers: one independent watchdog IWDT and one window watchdog WWDT
  - 1 24-bit autodecrement SysTick Timer
- **RTC**
  - Support calendar function
  - Alarm and regular wake-up from stop/standby mode
- **CRC computing unit**
- **96-bit unique device ID**
- **1 RNG**

Contents

2 Product Information

See the following table for APM32F425xG_F427xG product functions and peripheral configuration.

Table 1 Functions and Peripherals of APM32F425xG_F427xG Series Chips

Product		**APM32F427**					**APM32F425**				
Model(1)		CGUx	CGTx	RGTx	VGTx	ZGTx	CGUx	CGTx	RGTx	VGTx	ZGTx
Package		QFN48	LQFP48	LQFP64	LQFP100	LQFP144	QFN48	LQFP48	LQFP64	LQFP100	LQFP144
Core and maximum working frequency		Arm® 32-bit Cortex®-M4F@240MHz									
Working voltage		1.8~3.6V									
Flash(KB)		1024									
System + backup SRAM(KB)		448+4					192+4				
SMC		0				1	0				1
DMC		0				1	0				1
GPIOs		37		51	82	114	37		51	82	114
Communication interface	USART /UART	4/1		4/2			4/1		4/2		
	SPI	3									
	I2C	2		3			2		3		
	OTG_FS	2									
	CAN	2									
	QSPI	1									
	Ethernet	0		1			0		1		
	SDIO	0		1			0		1		
Timer	16-bit advanced	2									
	32-bit general	4									
	16-bit general	6									
	16-bit basic	2									
	System tick timer	1									
	Watchdog	2									
Real-time clock		1									
RNG		1									
12-bit ADC	Unit	3									
	External channel	10		16		24	10		16		24

Product		APM32F427	APM32F425
12-bit DAC	Unit	2	
	Channel	2	
Operating temperature		Ambient temperature: -40°Cto 85°C/-40°C to 105°C Junction temperature: -40°C to 105°C/-40°C to 125°C	

Note: (1) When x=6, ambient temperature is from -40°C to 85°C, and junction temperature is from -40°C to 105°C. When x=7, ambient temperature is from -40°C to 105°C, and junction temperature is from -40°C to 125°C.

3 Pin Information

3.1 Pin distribution

Figure 1 Distribution Diagram of APM32F425xG_F427xG Series LQFP144 Pins

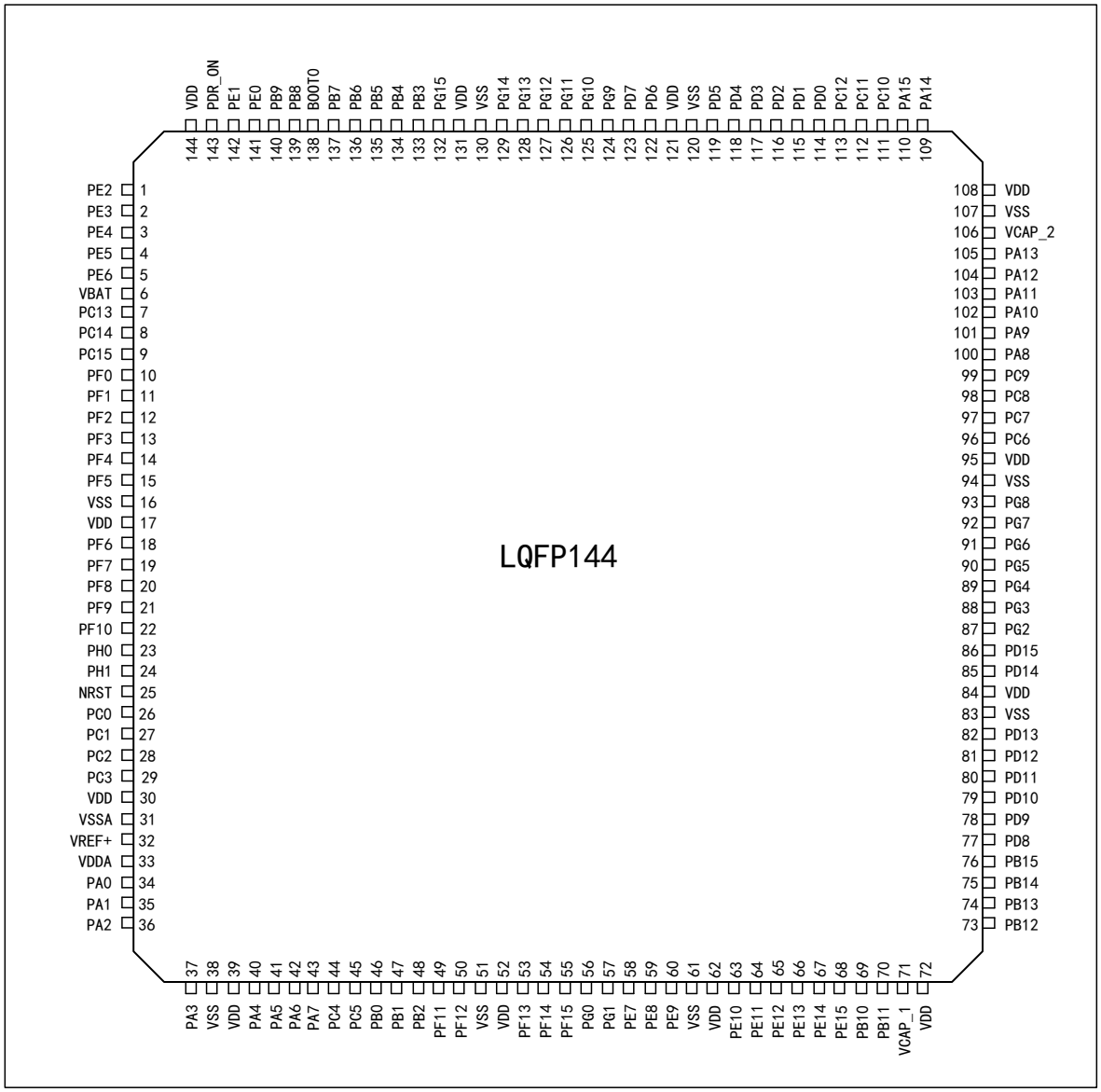


Figure 2 Distribution Diagram of APM32F425xG_F427xG Series LQFP100 Pins

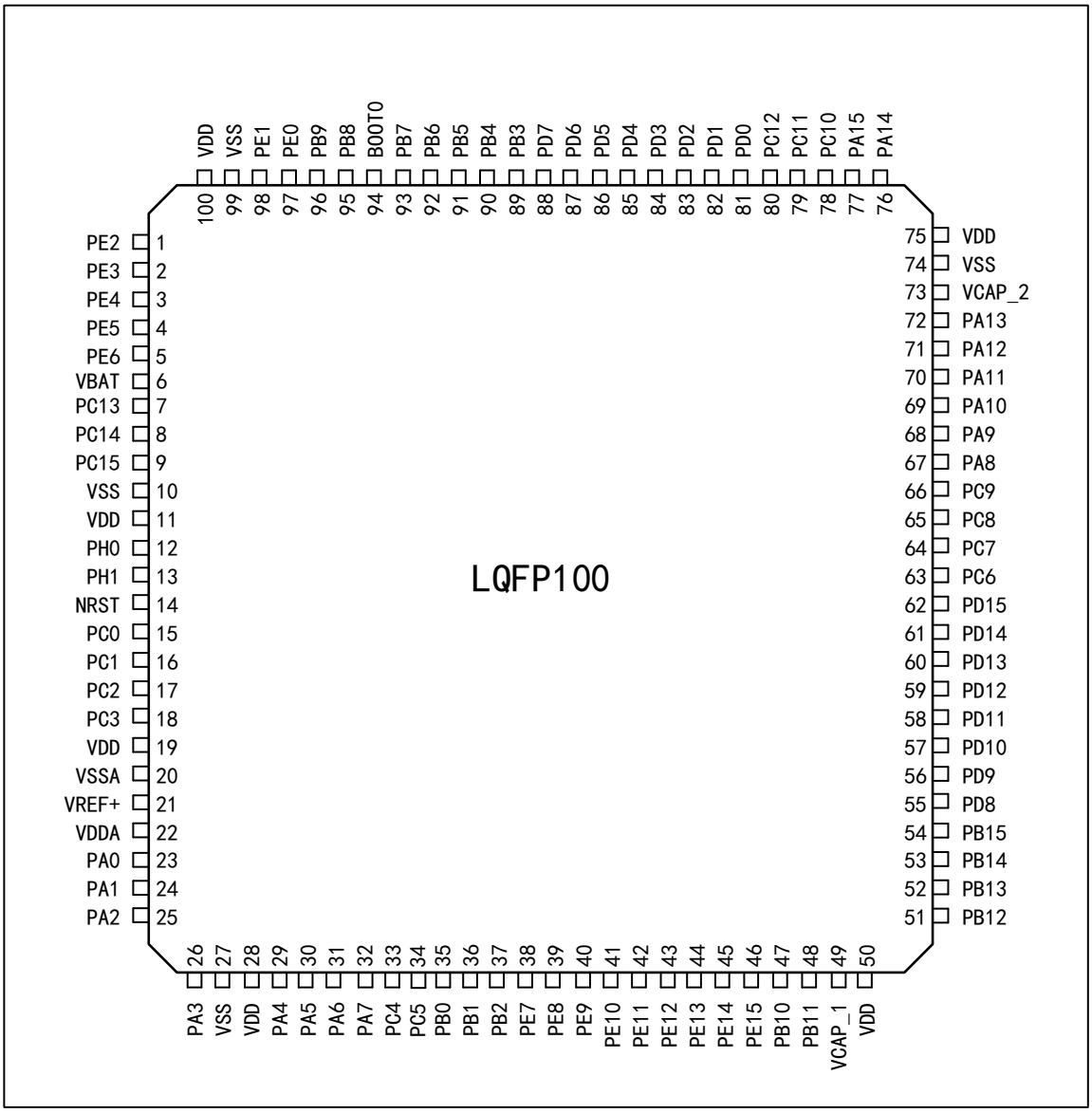


Figure 3 Distribution Diagram of APM32F425xG_F427xG Series LQFP64 Pins

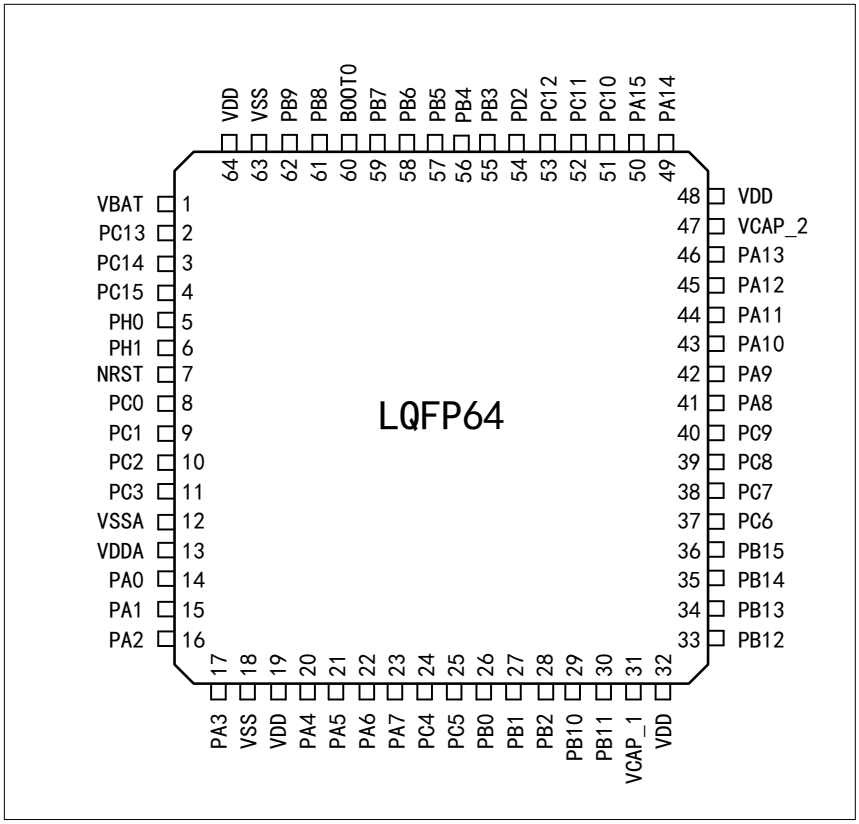


Figure 4 Distribution Diagram of APM32F425xG_F427xG Series LQFP48 Pins

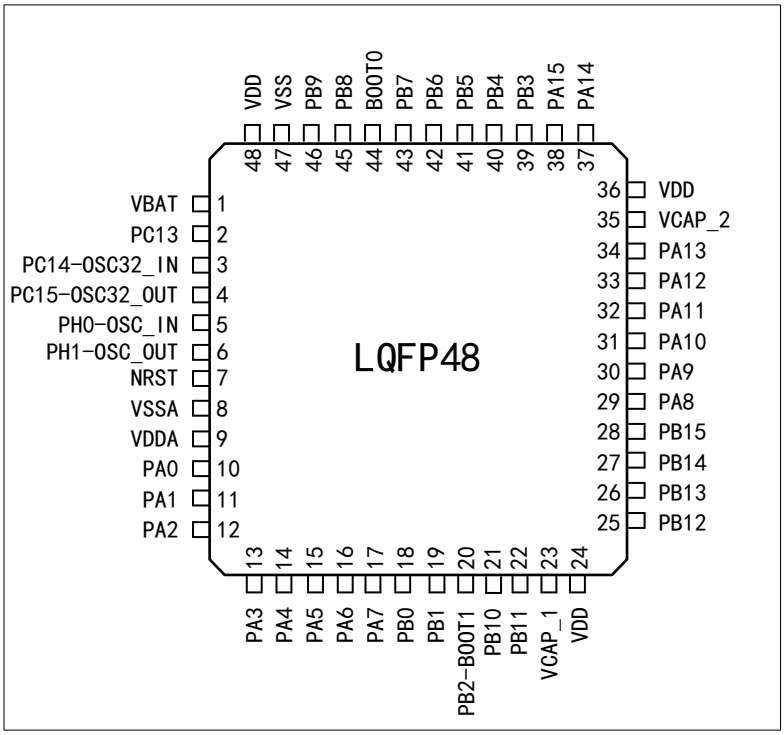
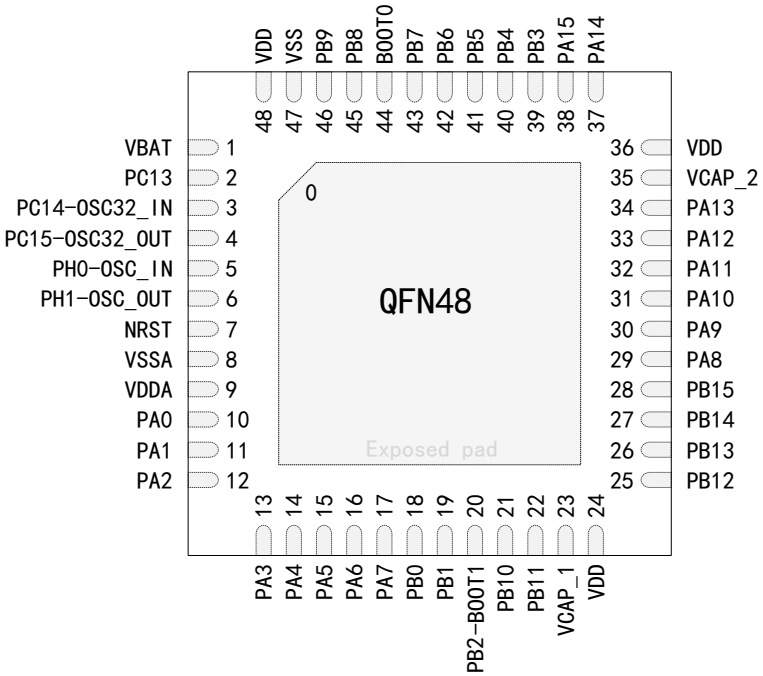


Figure 5 Distribution Diagram of APM32F425xG_F427xG Series QFN48 Pins



3.2 Pin function description

Table 2 Legends/Abbreviations Used in Output Pin Table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in parentheses below the pin name, the pin functions during and after reset are the same as the actual pin name	
Pin type		P	Power pin
		I	Only input pin
		I/O	I/O pin
I/O structure		5T	5V tolerant I/O (FT I/O)
		STDA	3.3V standard I/O, directly connected to ADC
		STD	3.3V standard I/O
		B	Dedicated Boot0 pin
		RST	Bidirectional reset pin with built-in pull-up resistor
Notes		Unless otherwise specified, all I/O pins are set as floating input during and after reset	
Pin function	Default multiplexing function	Function directly selected/enabled through peripheral register	
	Redefining function	Select this function through AFIO remapping register	

Table 3 Description of APM32F425xG_F427xG by Pin Number

Name (Function after reset)	Type	Structure	Multiplexing function	Additional function	QFN 48	LQFP 48	LQFP 64	LQFP 100	LQFP 144
PE2	I/O	5T	TRACECK, SMC_A23, ETH_MII_TXD3, EVENTOUT QSPI1_IO2	-	-	-	-	1	1
PE3	I/O	5T	TRACED0, SMC_A19, EVENTOUT	-	-	-	-	2	2
PE4	I/O	5T	TRACED1, SMC_A20, EVENTOUT	-	-	-	-	3	3
PE5	I/O	5T	TRACED2, SMC_A21, TMR9_CH1, EVENTOUT	-	-	-	-	4	4
PE6	I/O	5T	TRACED3, SMC_A22, TMR9_CH2, EVENTOUT	-	-	-	-	5	5
VBAT	P	-	-	-	1	1	1	6	6
PC13(1)	I/O	5T	EVENTOUT	RTC_OUT, RTC_TAMP1, RTC_TS	2	2	2	7	7
PC14-OSC32_IN（PC14）(1)	I/O	5T	EVENTOUT	OSC32_IN	3	3	3	8	8
PC15-OSC32_OUT（PC15）(1)	I/O	5T	EVENTOUT	OSC32_OUT	4	4	4	9	9
PF0	I/O	5T	SMC_A0, DMC_A0, I2C2_SDA, EVENTOUT	-	-	-	-	-	10
PF1	I/O	5T	SMC_A1, DMC_A1, I2C2_SCL, EVENTOUT	-	-	-	-	-	11
PF2	I/O	5T	SMC_A2,	-	-	-	-	-	12

Name (Function after reset)	Type	Structure	Multiplexing function	Additional function	QFN 48	LQFP 48	LQFP 64	LQFP 100	LQFP 144
			DMC_A2, I2C2_SMBA, EVENTOUT						
PF3	I/O	5T	SMC_A3, DMC_A3, EVENTOUT	ADC3_IN9	-	-	-	-	13
PF4	I/O	5T	SMC_A4, DMC_A4, EVENTOUT	ADC3_IN14	-	-	-	-	14
PF5	I/O	5T	SMC_A5, DMC_A5, EVENTOUT	ADC3_IN15	-	-	-	-	15
VSS	P	-	-	-	-	-	-	10	16
VDD	P	-	-	-	-	-	-	11	17
PF6	I/O	5T	TMR10_CH1, SMC_NIORD, QSPI1_IO3 EVENTOUT	ADC3_IN4	-	-	-	-	18
PF7	I/O	5T	TMR11_CH1, SMC_NREG, QSPI1_IO2 EVENTOUT	ADC3_IN5	-	-	-	-	19
PF8	I/O	5T	TMR13_CH1, SMC_NIOWR, QSPI1_IO0 EVENTOUT	ADC3_IN6	-	-	-	-	20
PF9	I/O	5T	TMR14_CH1, SMC_CD, QSPI1_IO1 EVENTOUT	ADC3_IN7	-	-	-	-	21
PF10	I/O	5T	SMC_INTR, QSPI1_SCK EVENTOUT	ADC3_IN8	-	-	-	-	22
PH0-OSC_IN (PH0)	I/O	5T	EVENTOUT	OSC_IN	5	5	5	12	23
PH1-OSC_OUT (PH1)	I/O	5T	EVENTOUT	OSC_OUT	6	6	6	13	24
NRST	I/O	RST	-	-	7	7	7	14	25

Name (Function after reset)	Type	Structure	Multiplexing function	Additional function	QFN 48	LQFP 48	LQFP 64	LQFP 100	LQFP 144
PC0	I/O	5T	DMC_WE EVENTOUT	ADC123_IN 10	-	-	8	15	26
PC1	I/O	5T	ETH_MDC, EVENTOUT	ADC123_IN 11	-	-	9	16	27
PC2	I/O	5T	SPI2_MISO, ETH_MII_TXD2, DMC_CS EVENTOUT	ADC123_IN 12	-	-	10	17	28
PC3	I/O	5T	SPI2_MOSI, ETH_MII_TX_CLK, DMC_CKE EVENTOUT	ADC123_IN 13	-	-	11	18	29
VDD	P	-	-	-	-	-	-	19	30
VSSA	P	-	-	-	8	8	12	20	31
VREF+	P	-	-	-	-	-	-	21	32
VDDA	P	-	-	-	9	9	13	22	33
PA0	I/O	5T	USART2_CTS, UART4_TX, ETH_MII_CRS, TMR2_CH1_ETR, TMR5_CH1, TMR8_ETR, EVENTOUT	WKUP, ADC123_IN 0	10	10	14	23	34
PA1	I/O	5T	USART2_RTS, UART4_RX, ETH_RMII_REF_CLK, ETH_MII_RX_CLK, TMR5_CH2, TMR2_CH2, QSPI1_IO3， EVENTOUT	ADC123_IN 1	11	11	15	24	35
PA2	I/O	5T	USART2_TX, TMR5_CH3, TMR9_CH1, TMR2_CH3,	ADC123_IN 2	12	12	16	25	36

Name (Function after reset)	Type	Structure	Multiplexing function	Additional function	QFN 48	LQFP 48	LQFP 64	LQFP 100	LQFP 144
			ETH_MDIO, EVENTOUT						
PA3	I/O	5T	USART2_RX, TMR5_CH4, TMR9_CH2, TMR2_CH4, ETH_MII_COL, EVENTOUT,	ADC123_IN3	13	13	17	26	37
VSS	P	-	-	-	-	-	18	27	38
VDD	P	-	-	-	-	-	19	28	39
PA4	I/O	5T	SPI1_NSS, SPI3_NSS, USART2_CK, OTG_FS2_SOF, EVENTOUT	DAC_OUT1, ADC12_IN4	14	14	20	29	40
PA5	I/O	5T	SPI1_SCK, TMR2_CH1_ETR, TMR8_CH1N, EVENTOUT	DAC_OUT2, ADC12_IN5	15	15	21	30	41
PA6	I/O	5T	SPI1_MISO, TMR8_BKIN, TMR13_CH1, TMR3_CH1, TMR1_BKIN, QSPI1_IO0，EVENTOUT	ADC12_IN6	16	16	22	31	42
PA7	I/O	5T	SPI1_MOSI, TMR8_CH1N, TMR14_CH1, TMR3_CH2, ETH_MII_RX_DV, TMR1_CH1N, ETH_RMII_CRS_DV, QSPI1_IO1，EVENTOUT	ADC12_IN7	17	17	23	32	43
PC4	I/O	5T	ETH_RMII_RX_D0,	ADC12_IN14	-	-	24	33	44

Name (Function after reset)	Type	Structure	Multiplexing function	Additional function	QFN 48	LQFP 48	LQFP 64	LQFP 100	LQFP 144
			ETH_MII_RX_D0, QSPI1_IO2, EVENTOUT						
PC5	I/O	5T	ETH_RMII_RX_D1, ETH_MII_RX_D1, QSPI1_IO3, EVENTOUT	ADC12_IN15	-	-	25	34	45
PB0	I/O	5T	TMR3_CH3 TMR8_CH2N, ETH_MII_RXD2, TMR1_CH2N, QSPI1_IO0，EVENTOUT	ADC12_IN8	18	18	26	35	46
PB1	I/O	5T	TMR3_CH4 TMR8_CH3N, ETH_MII_RXD3, TMR1_CH3N, QSPI1_SCK，EVENTOUT	ADC12_IN9	19	19	27	36	47
PB2-BOOT1 (PB2)	I/O	5T	QSPI1_SCK，EVENTOUT	-	20	20	28	37	48
PF11	I/O	5T	DMC_RAS，EVENTOUT	-	-	-	-	-	49
PF12	I/O	5T	SMC_A6, DMC_A6, EVENTOUT	-	-	-	-	-	50
VSS	P	-	-	-	-	-	-	-	51
VDD	P	-	-	-	-	-	-	-	52
PF13	I/O	5T	SMC_A7, DMC_A7, EVENTOUT	-	-	-	-	-	53
PF14	I/O	5T	SMC_A8, DMC_A8, EVENTOUT	-	-	-	-	-	54
PF15	I/O	5T	SMC_A9, DMC_A9, EVENTOUT	-	-	-	-	-	55

Name (Function after reset)	Type	Structure	Multiplexing function	Additional function	QFN 48	LQFP 48	LQFP 64	LQFP 100	LQFP 144
PG0	I/O	5T	SMC_A10, DMC_A10, EVENTOUT	-	-	-	-	-	56
PG1	I/O	5T	SMC_A11, DMC_A11, EVENTOUT	-	-	-	-	-	57
PE7	I/O	5T	SMC_D4, DMC_DQ4, TMR1_ETR, EVENTOUT	-	-	-	-	38	58
PE8	I/O	5T	SMC_D5, DMC_DQ5, TMR1_CH1N, EVENTOUT	-	-	-	-	39	59
PE9	I/O	5T	SMC_D6, DMC_DQ6, TMR1_CH1, EVENTOUT	-	-	-	-	40	60
VSS	P	-	-	-	-	-	-	-	61
VDD	P	-	-	-	-	-	-	-	62
PE10	I/O	5T	SMC_D7, DMC_DQ7, TMR1_CH2N, EVENTOUT	-	-	-	-	41	63
PE11	I/O	5T	SMC_D8, DMC_DQ8, TMR1_CH2, EVENTOUT	-	-	-	-	42	64
PE12	I/O	5T	SMC_D9, DMC_DQ9, TMR1_CH3N, EVENTOUT	-	-	-	-	43	65
PE13	I/O	5T	SMC_D10, DMC_DQ10, TMR1_CH3, EVENTOUT	-	-	-	-	44	66
PE14	I/O	5T	SMC_D11, DMC_DQ11, TMR1_CH4, EVENTOUT	-	-	-	-	45	67

Name (Function after reset)	Type	Structure	Multiplexing function	Additional function	QFN 48	LQFP 48	LQFP 64	LQFP 100	LQFP 144
PE15	I/O	5T	SMC_D12, DMC_DQ12, TMR1_BKIN, EVENTOUT	-	-	-	-	46	68
PB10	I/O	5T	SPI2_SCK, I2C2_SCL, USART3_TX, ETH_MII_RX_ER, TMR2_CH3, QSPI1_CS, QSPI1_IO1，EVENTOUT	-	21	21	29	47	69
PB11	I/O	5T	I2C2_SDA, USART3_RX, ETH_RMII_TX_EN, ETH_MII_TX_EN, TMR2_CH4, QSPI1_IO0，EVENTOUT	-	22	22	30	48	70
VCAP_1	P	-	-	-	23	23	31	49	71
VDD	P	-	-	-	24	24	32	50	72
PB12	I/O	5T	SPI2_NSS, I2C2_SMBAI, USART3_CK, TMR1_BKIN, CAN2_RX, ETH_RMII_TXD0, ETH_MII_TXD0, OTG_FS2_ID, EVENTOUT	-	25	25	33	51	73
PB13	I/O	5T	SPI2_SCK, USART3_CTS, TMR1_CH1N, CAN2_TX, ETH_RMII_TXD1,	OTG_FS2_VBUS	26	26	34	52	74

Name (Function after reset)	Type	Structure	Multiplexing function	Additional function	QFN 48	LQFP 48	LQFP 64	LQFP 100	LQFP 144
			ETH_MII_TXD1, EVENTOUT						
PB14	I/O	5T	SPI2_MISO, TMR1_CH2N, TMR12_CH1, OTG_FS2_DM, USART3_RTS, TMR8_CH2N, EVENTOUT	-	27	27	35	53	75
PB15	I/O	5T	SPI2_MOSI, TMR1_CH3N, TMR8_CH3N TMR12_CH2, OTG_FS2_DP, EVENTOUT	RTC_REFIN	28	28	36	54	76
PD8	I/O	5T	SMC_D13, DMC_DQ13, USART3_TX, EVENTOUT	-	-	-	-	55	77
PD9	I/O	5T	SMC_D14, DMC_DQ14, USART3_RX, EVENTOUT	-	-	-	-	56	78
PD10	I/O	5T	SMC_D15, DMC_DQ15, USART3_CK, EVENTOUT	-	-	-	-	57	79
PD11	I/O	5T	SMC_CLE, SMC_A16, USART3_CTS, QSPI1 _IO0，EVENTOUT	-	-	-	-	58	80
PD12	I/O	5T	SMC_ALE, SMC_A17, TMR4_CH1, USART3_RTS, QSPI1 _IO1，EVENTOUT	-	-	-	-	59	81
PD13	I/O	5T	SMC_A18, TMR4_CH2,	-	-	-	-	60	82

Name (Function after reset)	Type	Structure	Multiplexing function	Additional function	QFN 48	LQFP 48	LQFP 64	LQFP 100	LQFP 144
			QSPI1_IO3，EVENTOUT						
VSS	P	-	-	-	-	-	-	-	83
VDD	P	-	-	-	-	-	-	-	84
PD14	I/O	5T	SMC_D0, DMC_DQ0 TMR4_CH3, EVENTOUT	-	-	-	-	61	85
PD15	I/O	5T	SMC_D1, DMC_DQ1 TMR4_CH4, EVENTOUT	-	-	-	-	62	86
PG2	I/O	5T	SMC_A12, DMC_A12, EVENTOUT	-	-	-	-	-	87
PG3	I/O	5T	SMC_A13, DMC_A13, EVENTOUT	-	-	-	-	-	88
PG4	I/O	5T	SMC_A14, DMC_BA0 EVENTOUT	-	-	-	-	-	89
PG5	I/O	5T	SMC_A15, DMC_BA1 EVENTOUT	-	-	-	-	-	90
PG6	I/O	5T	SMC_INT2, QSPI1_CS，EVENTOUT	-	-	-	-	-	91
PG7	I/O	5T	SMC_INT3, USART6_CK, EVENTOUT	-	-	-	-	-	92
PG8	I/O	5T	DMC_CLK/CK USART6_RTS, ETH_PPS_OUT, EVENTOUT	-	-	-	-	-	93
VSS	P	-	-	-	-	-	-	-	94
VDD	P	-	-	-	-	-	-	-	95
PC6	I/O	5T	TMR8_CH1, SDIO_D6, USART6_TX,	-	-	-	37	63	96

Name (Function after reset)	Type	Structure	Multiplexing function	Additional function	QFN 48	LQFP 48	LQFP 64	LQFP 100	LQFP 144
			TMR3_CH1, EVENTOUT						
PC7	I/O	5T	TMR8_CH2, SDIO_D7, USART6_RX, TMR3_CH2, EVENTOUT	-	-	-	38	64	97
PC8	I/O	5T	TMR8_CH3, SDIO_D0, TMR3_CH3, USART6_CK, QSPI1_IO2，EVENTOUT	-	-	-	39	65	98
PC9	I/O	5T	MCO2, TMR8_CH4, SDIO_D1, I2C3_SDA, TMR3_CH4, QSPI1_IO0，EVENTOUT	-	-	-	40	66	99
PA8	I/O	5T	USART1_CK, TMR1_CH1, MCO, I2C3_SCL, OTG_FS1_SOF, EVENTOUT	-	29	29	41	67	100
PA9	I/O	5T	USART1_TX, TMR1_CH2, I2C3_SMBAI, EVENTOUT	OTG_FS1_VBUS	30	30	42	68	101
PA10	I/O	5T	USART1_RX, TMR1_CH3, OTG_FS1_ID, EVENTOUT	-	31	31	43	69	102
PA11	I/O	5T	USART1_CTS, CAN1_RX, TMR1_CH4, OTG_FS1_DM, EVENTOUT	-	32	32	44	70	103
PA12	I/O	5T	USART1_RTS,	-	33	33	45	71	104

Name (Function after reset)	Type	Structure	Multiplexing function	Additional function	QFN 48	LQFP 48	LQFP 64	LQFP 100	LQFP 144
			CAN1_TX, TMR1_ETR, OTG_FS1_DP, EVENTOUT						
PA13 (JTMS-SWDIO)	I/O	5T	JTMS-SWDIO, EVENTOUT	PA13	34	34	46	72	105
VCAP_2	P	-	-	-	35	35	47	73	106
VSS	P	-	-	-	-	-	-	74	107
VDD	P	-	-	-	36	36	48	75	108
PA14 (JTCK/SWCLK)	I/O	5T	JTCK-SWCLK, EVENTOUT	-	37	37	49	76	109
PA15 (JTDI)	I/O	5T	JTDI, SPI3_NSS, TMR2_CH1_ETR, SPI1_NSS, QSPI1_IO2，EVENTOUT	-	38	38	50	77	110
PC10	I/O	5T	SPI3_SCK, UART4_TX, SDIO_D2, USART3_TX, QSPI1_IO1，EVENTOUT	-	-	-	51	78	111
PC11	I/O	5T	UART4_RX, SPI3_MISO, SDIO_D3, USART3_RX, QSPI1_CS，EVENTOUT	-	-	-	52	79	112
PC12	I/O	5T	UART5_TX, SDIO_CK, SPI3_MOSI, USART3_CK, EVENTOUT	-	-	-	53	80	113
PD0	I/O	5T	SMC_D2, DMC_DQ2, CAN1_RX, EVENTOUT	-	-	-	-	81	114

Name (Function after reset)	Type	Structure	Multiplexing function	Additional function	QFN 48	LQFP 48	LQFP 64	LQFP 100	LQFP 144
PD1	I/O	5T	SMC_D3, DMC_DQ3, CAN1_TX, EVENTOUT	-	-	-	-	82	115
PD2	I/O	5T	TMR3_ETR, UART5_RX, SDIO_CMD, EVENTOUT	-	-	-	54	83	116
PD3	I/O	5T	SMC_CLK, USART2_CTS, QSPI1_SCK，EVENTOUT	-	-	-	-	84	117
PD4	I/O	5T	SMC_NOE, USART2_RTS, EVENTOUT	-	-	-	-	85	118
PD5	I/O	5T	SMC_NWE, USART2_TX, EVENTOUT	-	-	-	-	86	119
VSS	P	-	-	-	-	-	-	-	120
VDD	P	-	-	-	-	-	-	-	121
PD6	I/O	5T	SMC_NWAIT, USART2_RX, EVENTOUT	-	-	-	-	87	122
PD7	I/O	5T	SMC_NE1, SMC_NCE2, USART2_CK, EVENTOUT	-	-	-	-	88	123
PG9	I/O	5T	SMC_NE2, SMC_NCE3, USART6_RX, QSPI1_IO2，EVENTOUT	-	-	-	-	-	124
PG10	I/O	5T	SMC_NCE4_1, SMC_NE3, EVENTOUT	-	-	-	-	-	125
PG11	I/O	5T	SMC_NCE4_2, ETH_MII_TX_EN, ETH_RMII_TX_EN,	-	-	-	-	-	126

Name (Function after reset)	Type	Structure	Multiplexing function	Additional function	QFN 48	LQFP 48	LQFP 64	LQFP 100	LQFP 144
			EVENTOUT						
PG12	I/O	5T	SMC_NE4, USART6_RTS, EVENTOUT	-	-	-	-	-	127
PG13	I/O	5T	SMC_A24, USART6_CTS, ETH_MII_TXD0, ETH_RMII_TXD0, EVENTOUT	-	-	-	-	-	128
PG14	I/O	5T	SMC_A25, USART6_TX, ETH_MII_TXD1, ETH_RMII_TXD1, QSPI1_IO3，EVENTOUT	-	-	-	-	-	129
VSS	P	-	-	-	-	-	-	-	130
VDD	P	-	-	-	-	-	-	-	131
PG15	I/O	5T	DMC_CAS, USART6_CTS, EVENTOUT	-	-	-	-	-	132
PB3 (JTDO/TRACESWO)	I/O	5T	JTDO, TRACESWO, SPI3_SCK, TMR2_CH2, SPI1_SCK, QSPI1_IO3，EVENTOUT	-	39	39	55	89	133
PB4 (NJTRST)	I/O	5T	NJTRST, SPI3_MISO, TMR3_CH1, SPI1_MISO, EVENTOUT	-	40	40	56	90	134
PB5	I/O	5T	I2C1_SMBAI, CAN2_RX, ETH_PPS_OUT, TMR3_CH2, SPI1_MOSI,	-	41	41	57	91	135

Name (Function after reset)	Type	Structure	Multiplexing function	Additional function	QFN48	LQFP48	LQFP64	LQFP100	LQFP144
			SPI3_MOSI, EVENTOUT						
PB6	I/O	5T	I2C1_SCL, TMR4_CH1, CAN2_TX, USART1_TX, QSPI1_CS，EVENTOUT	-	42	42	58	92	136
PB7	I/O	5T	I2C1_SDA, SMC_NL, USART1_RX, TMR4_CH2, EVENTOUT	-	43	43	59	93	137
BOOT0	I	5T	-	VPP	44	44	60	94	138
PB8	I/O	5T	TMR4_CH3, SDIO_D4, TMR10_CH1, ETH_MII_TXD3, I2C1_SCL, CAN1_RX, EVENTOUT	-	45	45	61	95	139
PB9	I/O	5T	SPI2_NSS, TMR4_CH4, TMR11_CH1, SDIO_D5, I2C1_SDA, CAN1_TX, QSPI1_CS，EVENTOUT	-	46	46	62	96	140
PE0	I/O	5T	TMR4_ETR, SMC_NBL0, DMC_LDQM, EVENTOUT	-	-	-	-	97	141
PE1	I/O	5T	SMC_NBL1, DMC_UDQM, EVENTOUT	-	-	-	-	98	142
VSS	P	-	-	-	47	47	63	99	-
PDR_ON	I	5T	-	-	-	-	-	-	143
VDD	P	-	-	-	48	48	64	100	144

Note:

(1) PC13, PC14 and PC15 are powered through the power switch. As the switch only absorbs a limited current (3mA), the use of GPIO from PC13 to PC15 in output mode is limited:

① When the load is 30pF, the speed shall not exceed 2MHz.

② Not used for current source (for example, driving LED).

3.3 GPIO multiplexing function configuration

Table 4 GPIOA Multiplexing Function Configuration

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PA0	-	TMR2_CH1_ETR	TMR5_CH1	TMR8_ETR	-	-	-	USART2_CTS	UART4_TX	-	-	ETH_MII_CRS	-	-	-	EVENTOUT
PA1	-	TMR2_CH2	TMR5_CH2	-	-	-	-	USART2_RTS	UART4_RX	QSPI1_IO3	-	ETH_MII_RX_CLK ETH_RMII_REF_CLK	-	-	-	EVENTOUT
PA2	-	TMR2_CH3	TMR5_CH3	TMR9_CH1	-	-	-	USART2_TX	-	-	-	ETH_MDIO	-	-	-	EVENTOUT
PA3	-	TMR2_CH4	TMR5_CH4	TMR9_CH2	-	-	-	USART2_RX	-	-	-	ETH_MII_COL	-	-	-	EVENTOUT
PA4	-	-	-	-	-	SPI1_NSS	SPI3_NSS	USART2_CK	-	-	-	-	OTG_FS2_SOF	-	-	EVENTOUT
PA5	-	TMR2_CH1_ETR	-	TMR8_CH1N	-	SPI1_SCK	-	-	-	-	-	-	-	-	-	EVENTOUT
PA6	-	TMR1_BKIN	TMR3_CH1	TMR8_BKIN	-	SPI1_MISO	-	-	-	TMR13_CH1	QSPI1_IO0	-	-	-	-	EVENTOUT
PA7	-	TMR1_CH1N	TMR3_CH2	TMR8_CH1N	-	SPI1_MOSI	-	-	-	TMR14_CH1	QSPI1_IO1	ETH_MII_RX_DV ETH_RMII_CRS_DV	-	-	-	EVENTOUT
PA8	MCO1	TMR1_CH1	-	-	I2C3_SCL	-	-	USART1_CK	-	-	OTG_FS1_SOF	-	-	-	-	EVENTOUT

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PA9	-	TMR1_CH2	-	-	I2C3_SMBA	-	-	USART1_TX	-	-	-	-	-	-	-	EVENTOUT
PA10	-	TMR1_CH3	-	-	-	-	-	USART1_RX	-	-	OTG_FS1_ID	-	-	-	-	EVENTOUT
PA11	-	TMR1_CH4	-	-	-	-	-	USART1_CTS	-	CAN1_RX	OTG_FS1_DM	-	-	-	-	EVENTOUT
PA12	-	TMR1_ETR	-	-	-	-	-	USART1_RTS	-	CAN1_TX	OTG_FS1_DP	-	-	-	-	EVENTOUT
PA13	JTMS_SWDIO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
PA14	JTCK_SWCLK	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
PA15	JTDI	TMR2_CH1 TMR2_ETR	-	-	-	SPI1_NSS	SPI3_NSS I2C3_WS	-	-	-	QSPI1_IO2	-	-	-	-	EVENTOUT

Table 5 GPIOB Multiplexing Function Configuration

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PB0	-	TMR1_CH2N	TMR3_CH3	TMR8_CH2N	-	-	-	-	-	QSPI1_IO0	-	ETH_MII_RXD2	-	-	-	EVENTOUT

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PB1	-	TMR1_CH3N	TMR3_CH4	TMR8_CH3N	-	-	-	-	-	QSPI1_SCK	-	ETH_MII_RXD3	-	-	-	EVENTOUT
PB2	-	-	-	-	-	-	-	-	-	QSPI1_SCK	-	-	-	-	-	EVENTOUT
PB3	JTDO/TRACESWO	TMR2_CH2	-	-	-	SPI1_SCK	SPI3_SCK	-	-	QSPI1_IO3	-	-	-	-	-	EVENTOUT
PB4	NJTRST	-	TMR3_CH1	-	-	SPI1_MISO	SPI3_MISO	-	-	-	-	-	-	-	-	EVENTOUT
PB5	-	-	TMR3_CH2	-	I2C1_SMBA	SPI1_MOSI	SPI3_MOSI	-	-	CAN2_RX	-	ETH_PPS_OUT	-	-	-	EVENTOUT
PB6	-	-	TMR4_CH1	-	I2C1_SCL	-	-	USART1_TX	-	CAN2_TX	QSPI1_CS	-	-	-	-	EVENTOUT
PB7	-	-	TMR4_CH2	-	I2C1_SDA	-	-	USART1_RX	-	-	-	-	SMC_NL	-		EVENTOUT
PB8	-	-	TMR4_CH3	TMR10_CH1	I2C1_SCL	-	-	-	-	CAN1_RX	-	ETH_MII_TXD3	SDIO_D4	-	-	EVENTOUT
PB9	-	-	TMR4_CH4	TMR11_CH1	I2C1_SDA	SPI2_NSS	-	-	-	CAN1_TX	QSPI1_CS	-	SDIO_D5	-	-	EVENTOUT
PB10	-	TMR2_CH3	-	-	I2C2_SCL	SPI2_SCK	-	USART3_TX	-	QSPI1_CS	QSPI1_IO1	ETH_MII_RX_ER	-	-	-	EVENTOUT
PB11	-	TMR2_CH4	-	-	I2C2_SDA	-	-	USART3_RX	-	QSPI1_IO0	-	ETH_MII_TX_EN / ETH_RMII_TX_EN	-	-	-	EVENTOUT

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PB12	-	TMR1_BKIN	-	-	I2C2_SMBA	SPI2_NSS	-	USART3_CK	-	CAN2_RX	-	ETH_RMII_TXD0/ ETH_MII_TXD0	OTG_FS2_ID	-	-	EVENTOUT
PB13	-	TMR1_CH1N	-	-	-	SPI2_SCK	-	USART3_CTS	-	CAN2_TX	-	ETH_RMII_TXD1/ ETH_MII_TXD1	-	-	-	EVENTOUT
PB14	-	TMR1_CH2N	-	TMR8_CH2N	-	SPI2_MISO	-	USART3_RTS	-	TMR12_CH1	-	-	OTG_FS2_DM	-	-	EVENTOUT
PB15	RTC_REFIN	TMR1_CH3N	-	TMR8_CH3N	-	SPI2_MOSI	-	-	-	TMR12_CH2	-	-	OTG_FS2_DP	-	-	EVENTOUT

Table 6 GPIOC Multiplexing Function Configuration

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PC0	-	-	-	-	-	-	-	-	-	-	-	-	DMC_WE	-	-	EVENTOUT
PC1	-	-	-	-	-	-	-	-	-	-	-	ETH_MDC	-	-	-	EVENTOUT
PC2	-	-	-	-	-	SPI2_MISO	-	-	-	-	-	ETH_MII_TXD2	DMC_CS	-	-	EVENTOUT
PC3	-	-	-	-	-	SPI2_MOSI	-	-	-	-	-	ETH_MII_TX_CLK	DMC_CKE	-	-	EVENTOUT

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PC4	-	-	-	-	-	-	-	-	-	-	QSPI1_IO2	ETH_MII_RXD0 ETH_RMII_RXD0	-	-	-	EVENTOUT
PC5	-	-	-	-	-	-	-	-	-	-	QSPI1_IO3	ETH_MII_RXD1 ETH_RMII_RXD1	-	-	-	EVENTOUT
PC6	-	-	TMR3_CH1	TMR8_CH1	-	-	-	-	USART6_TX	-	-	-	SDIO_D6	-	-	EVENTOUT
PC7	-	-	TMR3_CH2	TMR8_CH2	-	-	-	-	USART6_RX	-	-	-	SDIO_D7	-	-	EVENTOUT
PC8	-	-	TMR3_CH3	TMR8_CH3	-	-	-	-	USART6_CK	-	QSPI1_IO2	-	SDIO_D0	-	-	EVENTOUT
PC9	MCO2	-	TMR3_CH4	TMR8_CH4	-	-	-	-	-	-	QSPI1_IO0	-	SDIO_D1	-	-	EVENTOUT
PC10	-	-	-	-	-	-	SPI3_SCK/	USART3_TX	UART4_TX	-	QSPI1_IO1	-	SDIO_D2	-	-	EVENTOUT
PC11	-	-	-	-	-	-	SPI3_MISO/	USART3_RX	UART4_RX	-	QSPI1_CS	-	SDIO_D3	-	-	EVENTOUT
PC12	-	-	-	-	-	-	SPI3_MOSI	USART3_CK	UART5_TX	-	-	-	SDIO_CK	-	-	EVENTOUT
PC13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT

Table 7 GPIOD Multiplexing Function Configuration

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PD0	-	-	-	-	-	-	-	-	-	CAN1_RX	-	-	SMC_D2 DMC_DQ2	-	-	EVENTOUT
PD1	-	-	-	-	-	-	-	-	-	CAN1_TX	-	-	SMC_D3 DMC_DQ3	-	-	EVENTOUT
PD2	-	-	TMR3_ETR	-	-	-	-	-	UART5_RX	-	-	-	SDIO_CMD	-	-	EVENTOUT
PD3	-	-	-	-	-	-	-	USART2_CTS	-	-	QSPI1_SCK	-	SMC_CLK	-	-	EVENTOUT
PD4	-	-	-	-	-	-	-	USART2_RTS	-	-	-	-	SMC_NOE	-	-	EVENTOUT
PD5	-	-	-	-	-	-	-	USART2_TX	-	-	-	-	SMC_NWE	-	-	EVENTOUT
PD6	-	-	-	-	-	-	-	USART2_RX	-	-	-	-	SMC_NWAIT	-	-	EVENTOUT
PD7	-	-	-	-	-	-	-	USART2_CK	-	-	-	-	SMC_NE1/SMC_NCE2	-	-	EVENTOUT
PD8	-	-	-	-	-	-	-	USART3_TX	-	-	-	-	SMC_D13 DMC_DQ13	-	-	EVENTOUT
PD9	-	-	-	-	-	-	-	USART3_RX	-	-	-	-	SMC_D14 DMC_DQ14	-	-	EVENTOUT
PD10	-	-	-	-	-	-	-	USART3_CK	-	-	-	-	SMC_D15 DMC_DQ15	-	-	EVENTOUT

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PD11	-	-	-	-	-	-	-	USART 3_CTS	-	-	QSPI1 _IO0	-	SMC_A16	-	-	EVENTOUT
PD12	-	-	TMR4_ CH1	-	-	-	-	USART 3_RTS	-	-	QSPI1 _IO1	-	SMC_A17	-	-	EVENTOUT
PD13	-	-	TMR4_ CH2	-	-	-	-	-	-	-	QSPI1_IO 3	-	SMC_A18	-	-	EVENTOUT
PD14	-	-	TMR4_ CH3	-	-	-	-	-	-	-	-	-	SMC_D0 DMC_DQ0	-	-	EVENTOUT
PD15	-	-	TMR4_ CH4	-	-	-	-	-	-	-	-	-	SMC_D1 DMC_DQ1	-	-	EVENTOUT

Table 8 GPIOE Multiplexing Function Configuration

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PE0	-	-	TMR4_ ETR	-	-	-	-	-	-	-	-	-	SMC_NBL0 DMC_LDQM	-	-	EVENTOUT
PE1	-	-	-	-	-	-	-	-	-	-	-	-	SMC_NBL1 DMC_UDQM	-	-	EVENTOUT
PE2	TRACE CLK	-	-	-	-	-	-	-	-	-	QSPI1 _IO2	ETH_MII _TXD3	SMC_A23	-	-	EVENTOUT
PE3	TRACE D0	-	-	-	-	-	-	-	-	-	-	-	SMC_A19	-	-	EVENTOUT
PE4	TRACE D1	-	-	-	-	-	-	-	-	-	-	-	SMC_A20	-	-	EVENTOUT
PE5	TRACE D2	-	-	TMR9 _CH1	-	-	-	-	-	-	-	-	SMC_A21	-	-	EVENTOUT
PE6	TRACE D3	-	-	TMR9 _CH2	-	-	-	-	-	-	-	-	SMC_A22	-	-	EVENTOUT

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PE7	-	TMR1_ETR	-	-	-	-	-	-	-	-	-	-	SMC_D4 DMC_DQ4	-	-	EVENTOUT
PE8	-	TMR1_CH1N	-	-	-	-	-	-	-	-	-	-	SMC_D5 DMC_DQ5	-	-	EVENTOUT
PE9	-	TMR1_CH1	-	-	-	-	-	-	-	-	-	-	SMC_D6 DMC_DQ6	-	-	EVENTOUT
PE10	-	TMR1_CH2N	-	-	-	-	-	-	-	-	-	-	SMC_D7 DMC_DQ7	-	-	EVENTOUT
PE11	-	TMR1_CH2	-	-	-	-	-	-	-	-	-	-	SMC_D8 DMC_DQ8	-	-	EVENTOUT
PE12	-	TMR1_CH3N	-	-	-	-	-	-	-	-	-	-	SMC_D9 DMC_DQ9	-	-	EVENTOUT
PE13	-	TMR1_CH3	-	-	-	-	-	-	-	-	-	-	SMC_D10 DMC_DQ10	-	-	EVENTOUT
PE14	-	TMR1_CH4	-	-	-	-	-	-	-	-	-	-	SMC_D11 DMC_DQ11	-	-	EVENTOUT
PE15	-	TMR1_BKIN	-	-	-	-	-	-	-	-	-	-	SMC_D12 DMC_DQ12	-	-	EVENTOUT

Table 9 GPIOF Multiplexing Function Configuration

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PF0	-	-	-	-	I2C2_SDA	-	-	-	-	-	-	-	SMC_A0 DMC_A0	-	-	EVENTOUT

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PF1	-	-	-	-	I2C2_SCL	-	-	-	-	-	-	-	SMC_A1 DMC_A1	-	-	EVENTOUT
PF2	-	-	-	-	I2C2_SMBA	-	-	-	-	-	-	-	SMC_A2 DMC_A2	-	-	EVENTOUT
PF3	-	-	-	-	-	-	-	-	-	-	-	-	SMC_A3 DMC_A3	-	-	EVENTOUT
PF4	-	-	-	-	-	-	-	-	-	-	-	-	SMC_A4 DMC_A4	-	-	EVENTOUT
PF5	-	-	-	-	-	-	-	-	-	-	-	-	SMC_A5 DMC_A5	-	-	EVENTOUT
PF6	-	-	-	TMR 10_C H1	-	-	-	-	-	-	QSPI1 _IO3	-	SMC_NIORD	-	-	EVENTOUT
PF7	-	-	-	TMR 11_C H1	-	-	-	-	-	-	QSPI1 _IO2	-	SMC_NREG	-	-	EVENTOUT
PF8	-	-	-	-	-	-	-	-	-	TMR13_CH 1	QSPI1 _IO0	-	SMC_NIOWR	-	-	EVENTOUT
PF9	-	-	-	-	-	-	-	-	-	TMR14_CH 1	QSPI1 _IO1	-	SMC_CD	-	-	EVENTOUT
PF10	-	-	-	-	-	-	-	-	-	-	QSPI1 _SCK	-	SMC_INTR	-	-	EVENTOUT
PF11	-	-	-	-	-	-	-	-	-	-	-	-	DMC_RAS	-	-	EVENTOUT
PF12	-	-	-	-	-	-	-	-	-	-	-	-	SMC_A6 DMC_A6	-	-	EVENTOUT
PF13	-	-	-	-	-	-	-	-	-	-	-	-	SMC_A7 DMC_A7	-	-	EVENTOUT

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PF14	-	-	-	-	-	-	-	-	-	-	-	-	SMC_A8 DMC_A8	-	-	EVENTOUT
PF15	-	-	-	-	-	-	-	-	-	-	-	-	SMC_A9 DMC_A9	-	-	EVENTOUT

Table 10 GPIOG Multiplexing Function Configuration

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PG0	-	-	-	-	-	-	-	-	-	-	-	-	SMC_A10 DMC_A10	-	-	EVENTOUT
PG1	-	-	-	-	-	-	-	-	-	-	-	-	SMC_A11 DMC_A11	-	-	EVENTOUT
PG2	-	-	-	-	-	-	-	-	-	-	-	-	SMC_A12 DMC_A12	-	-	EVENTOUT
PG3	-	-	-	-	-	-	-	-	-	-	-	-	SMC_A13 DMC_A13	-	-	EVENTOUT
PG4	-	-	-	-	-	-	-	-	-	-	-	-	SMC_A14 DMC_BA0	-	-	EVENTOUT
PG5	-	-	-	-	-	-	-	-	-	-	-	-	SMC_A15 DMC_BA1	-	-	EVENTOUT
PG6	-	-	-	-	-	-	-	-	-	-	QSPI1_CS	-	SMC_INT2	-	-	EVENTOUT
PG7	-	-	-	-	-	-	-	-	USART6 _CK	-	-	-	SMC_INT3	-	-	EVENTOUT
PG8	-	-	-	-	-	-	-	-	USART6 _RTS	-	-	ETH_PPS _OUT	DMC_CLK/CK	-	-	EVENTOUT
PG9	-	-	-	-	-	-	-	-	USART6 _RX	-	QSPI1_IO 2	-	SMC_NE2/SM C_NCE3	-	-	EVENTOUT

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PG10	-	-	-	-	-	-	-	-	-	-	-	-	SMC_NCE4_1 /SMC_NE3	-	-	EVENTOUT
PG11	-	-	-	-	-	-	-	-	-	-	-	ETH_MII_ TX_EN ETH_RMII _TX_EN	SMC_NCE4_2	-	-	EVENTOUT
PG12	-	-	-	-	-	-	-	-	USART6 _RTS	-	-	-	SMC_NE4	-	-	EVENTOUT
PG13	-	-	-	-	-	-	-	-	USART6 _CTS	-	-	ETH_MII_ TXD0 ETH_RMII _TXD0	SMC_A24	-	-	EVENTOUT
PG14	-	-	-	-	-	-	-	-	USART6 _TX	-	QSPI1_IO 3	ETH_MII_ TXD1 ETH_RMII _TXD1	SMC_A25	-	-	EVENTOUT
PG15	-	-	-	-	-	-	-	-	USART6 _CTS	-	-	-	DMC_CAS	-	-	EVENTOUT

Table 11 GPIOH Multiplexing Function Configuration

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PH0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
PH1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT

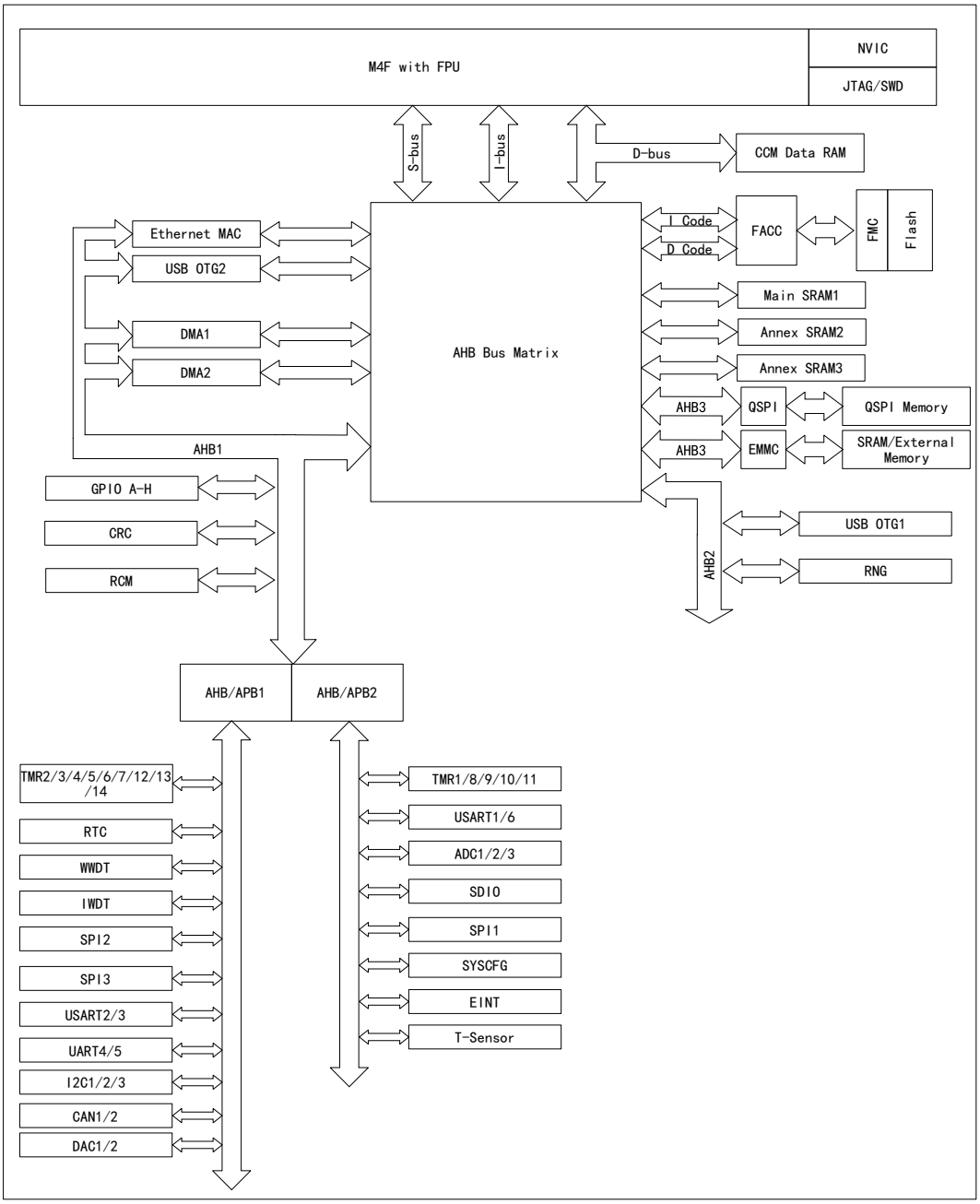
4 Function Description

This chapter mainly introduces the system architecture, interrupt, on-chip memory, clock, power supply and peripheral features of APM32F425xG_F427xG series products. For information about the Arm® Cortex®-M4F core, refer to the *Arm® Cortex®-M4F Technical Reference Manual*, which can be downloaded from Arm's website.

4.1 System architecture

4.1.1 System block diagram

Figure 6 APM32F425xG_F427xG System Block Diagram



4.1.2 Address mapping

Table 12 APM32F425xG_F427xG Series Address Mapping

Region	Start Address	Peripheral Name
Code	0x0000 0000	Code mapping area
Code	0x0800 0000	FLASH
Code	0x0810 0000	Reserved
CCM	0x1000 0000	CCM (SRAM)
Code	0x1001 0000	Reserved
Code	0x1FFF 0000	System memory area (ROM)
Code	0x1FFF 7800	OTP area
Code	0x1FFF 7A10	Reserved
Code	0x1FFF C000	Option bytes
Code	0x1FFF C010	Reserved
SRAM1+ SRAM1	0x2000 0000	SRAM
SRAM3	0x2002 0000	SRAM (APM32F427 supported)
—	0x2006 0000	Reserved
APB1 bus	0x4000 0000	TMR2
APB1 bus	0x4000 0400	TMR3
APB1 bus	0x4000 0800	TMR4
APB1 bus	0x4000 0C00	TMR5
APB1 bus	0x4000 1000	TMR6
APB1 bus	0x4000 1400	TMR7
APB1 bus	0x4000 1800	TMR12
APB1 bus	0x4000 1C00	TMR13
APB1 bus	0x4000 2000	TMR14
APB1 bus	0x4000 2400	Reserved
APB1 bus	0x4000 2800	RTC
APB1 bus	0x4000 2C00	WWDT
APB1 bus	0x4000 3000	IWDT
APB1 bus	0x4000 3800	SPI2
APB1 bus	0x4000 3C00	SPI3
APB1 bus	0x4000 4400	USART2
APB1 bus	0x4000 4800	USART3
APB1 bus	0x4000 4C00	UART4
APB1 bus	0x4000 5000	UART5
APB1 bus	0x4000 5400	I2C1
APB1 bus	0x4000 5800	I2C2
APB1 bus	0x4000 5C00	I2C3
APB1 bus	0x4000 6000	Reserved

Region	Start Address	Peripheral Name
APB1 bus	0x4000 6400	CAN1
APB1 bus	0x4000 6800	CAN2
APB1 bus	0x4000 6C00	Reserved
APB1 bus	0x4000 7000	PMU
APB1 bus	0x4000 7400	DAC
APB1 bus	0x4000 7800	Reserved
—	0x4000 8000	Reserved
APB2 bus	0x4001 0000	TMR1
APB2 bus	0x4001 0400	TMR8
APB2 bus	0x4001 0800	Reserved
APB2 bus	0x4001 1000	USART1
APB2 bus	0x4001 1400	USART6
APB2 bus	0x4001 1800	Reserved
APB2 bus	0x4001 2000	ADC1/2/3
APB2 bus	0x4001 2400	Reserved
APB2 bus	0x4001 2C00	SDI0
APB2 bus	0x4001 3000	SPI1
APB2 bus	0x4001 3400	Reserved
APB2 bus	0x4001 3800	SYSCFG
APB2 bus	0x4001 3C00	EINT
APB2 bus	0x4001 4000	TMR9
APB2 bus	0x4001 4400	TMR10
APB2 bus	0x4001 4800	TMR11
APB2 bus	0x4001 4C00	Reserved
—	0x4001 5800	Reserved
AHB bus	0x4002 0000	GPIOA
AHB bus	0x4002 0400	GPIOB
AHB bus	0x4002 0800	GPIOC
AHB bus	0x4002 0C00	GPIOD
AHB bus	0x4002 1000	GPIOE
AHB bus	0x4002 1400	GPIOF
AHB bus	0x4002 1800	GPIOG
AHB bus	0x4002 1C00	GPIOH
AHB bus	0x4002 2400	Reserved
AHB bus	0x4002 3000	CRC
AHB bus	0x4002 3400	Reserved
AHB bus	0x4002 3800	RCM
AHB bus	0x4002 3C00	FMC

Region	Start Address	Peripheral Name
AHB bus	0x4002 4000	Back up SRAM
AHB bus	0x4002 5000	Reserved
AHB bus	0x4002 6000	DMA1
AHB bus	0x4002 6400	DMA2
AHB bus	0x4002 6800	Reserved
AHB bus	0x4002 8000	MAC
AHB bus	0x4002 9400	Reserved
AHB bus	0x4004 0000	USB OTG_FS2
AHB bus	0x4008 0000	Reserved
AHB bus	0x5000 0000	USB OTG_FS1
AHB bus	0x5004 0000	Reserved
AHB bus	0x5005 0400	Reserved
AHB bus	0x5006 0800	RNG
AHB bus	0x5006 0C00	Reserved
AHB bus	0x6000 0000	EMMC bank 1 NOR/PSRAM 1/SDRA
AHB bus	0x6400 0000	EMMC bank 1 NOR/PSRAM 2/SDRA
AHB bus	0x6800 0000	EMMC bank 1 NOR/PSRAM 3/SDRA
AHB bus	0x6C00 0000	EMMC bank 1 NOR/PSRAM 4/SDRA
AHB bus	0x7000 0000	EMMC bank 2 NAND (NAND1)
AHB bus	0x8000 0000	EMMC bank 3 NAND (NAND2)
AHB bus	0x9000 0000	PCCARD/QSPI
AHB bus	0xA000 0000	EMMC
AHB bus	0xA000 1000	QSPI
—	0xB000 0000	Reserved
—	0xC000 0000	Reserved
Core	0xE000 0000	Core peripheral
—	0xE010 0000	Reserved

4.1.3 Startup configuration

At startup, the user can select one of the following three startup modes by setting the high and low levels of the Boot pin:

- Startup from main memory
- Startup from BootLoader
- Startup from built-in SRAM

The user can use serial interface to reprogram the user Flash if starting up from BootLoader.

4.2 Core

The core of APM32F425xG_F427xG is Arm® Cortex®-M4F with FPU computing unit. Based on

this platform, the development cost is low and the power consumption is low. It can provide excellent computing performance and advanced system interrupt response, and is compatible with all Arm tools and software.

4.3 Interrupt controller

4.3.1 Nested Vector Interrupt Controller (NVIC)

It embeds a nested vectored interrupt controller (NVIC) that can handle up to 88 maskable interrupt channels (not including 16 interrupt lines of Cortex®-M4F) and 16 priority levels. The interrupt vector entry address can be directly transmitted to the core, so that the interrupt response processing with low delay can give priority to the late higher priority interrupt.

4.3.2 External Interrupt/Event Controller (EINT)

The external interrupt/event controller consists of 23 edge detectors, and each detector includes edge detection circuit and interrupt/event request generation circuit. Each detector can be configured as rising edge trigger, falling edge trigger or both and can be masked independently. Up to 114 GPIOs can be connected to 16 external interrupt lines.

4.4 On-chip memory

On-chip memory includes main memory area, SRAM and information block. The information block includes system memory area and option byte; the system memory area stores BootLoader, 96-bit unique device ID and capacity information of main memory area; the system memory area has been written into the program when leaving the factory and cannot be erased.

Table 13 On-chip Memory Area

Memory	Maximum capacity	Function
Main memory area	1MB	Store user programs and data
SRAM	(448+4)KB	CPU can access at 0 wait cycle (read/write)
System memory area	30KB	Store BootLoader, 96-bit unique device ID, and main memory area capacity information
Option byte	16Bytes	Configure read-write protection for the main memory area, MCU working mode

4.4.1 Configurable external memory controller (EMMC)

APM32F425xG_F427xG series integrate EMMC module, consists of SMC (Static Memory Controller), DMC (Dynamic Memory Controller), and supports PC card, SRAM, SDRAM, PSRAM, NorFlash and NandFlash.

Function introduction:

- Three EMMC interrupt sources, connected to NVIC unit through logic OR
- Write FIFO
- The code can run in off-chip memories except NAND flash and PC card
- Connect to LCD

4.4.2 LCD parallel interface (LCD)

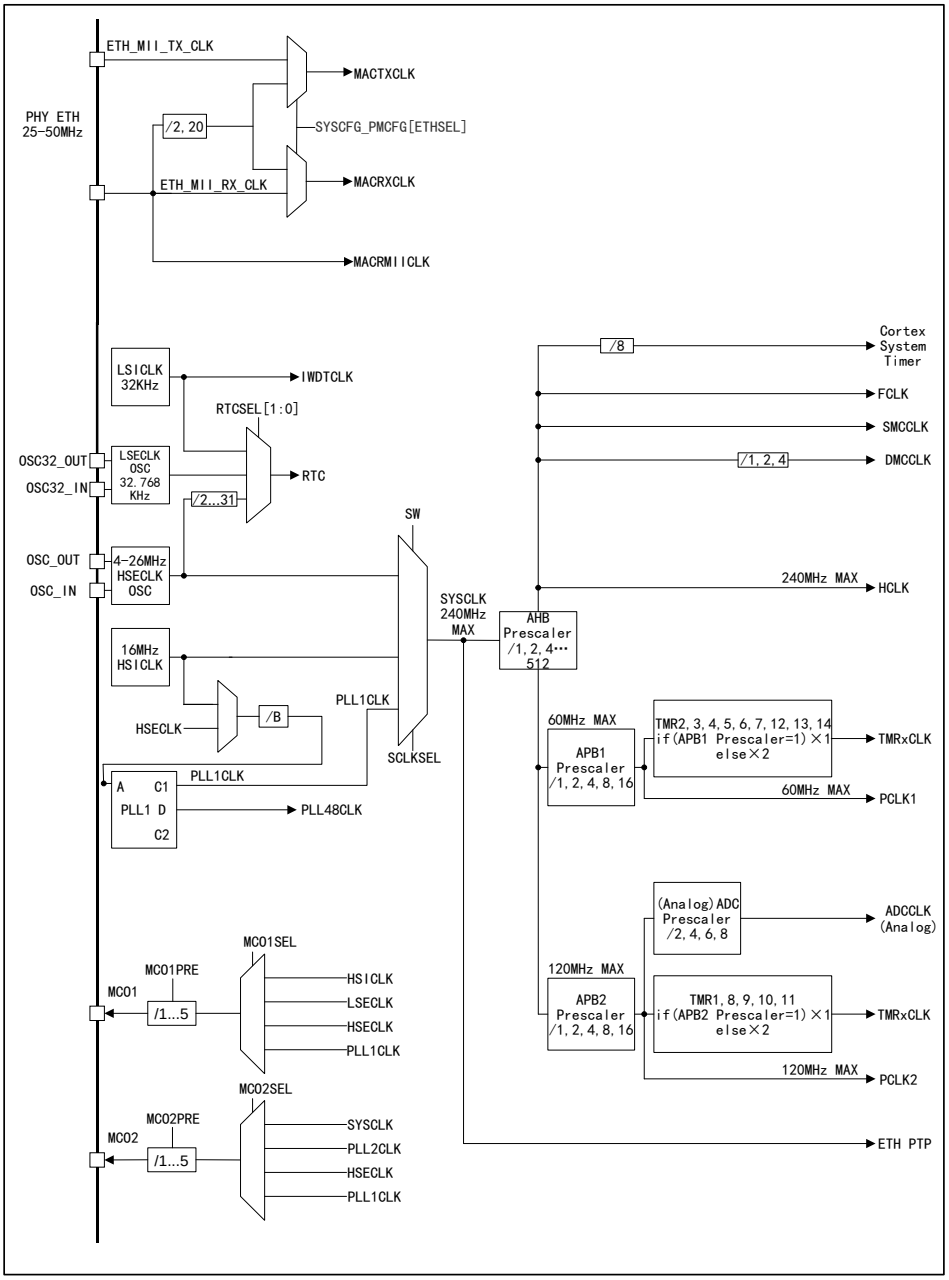
EMMC can be configured to seamlessly connection with most graphic LCD controllers, and supports the modes of Intel 8080 and Motorola 6800, and can flexibly connect with specific LCD interface. This LCD parallel interface can be used to easily build a simple graphics application environment or implement a high-performance scheme with a dedicated acceleration controller.

4.5 Clock

4.5.1 Clock tree

Clock tree of APM32F425xG_F427xG is shown in the figure below:

Figure 7 APM32F425xG_F427xG Clock Tree



4.5.2 Clock source

Clock source is divided into high-speed clock and low-speed clock according to the speed. The high-speed clock includes HSICLK and HSECLK, and the low-speed clock includes LSECLK and LSICLK. Besides, some modules may have additional clock source pins to obtain the required clock frequency through external circuits.

4.5.3 System clock

HSICLK, PLL1CLK and HSECLK can be selected as system clock. The clock source of PLL1CLK can be HSICLK or HSECLK. The required system clock can be obtained by configuring PLL clock multiplier factor and division factor.

When the product is reset and started, HSICLK is selected as the system clock by default, and then the user can choose one of the above clock sources as the system clock. When HSECLK failure is detected, the system will automatically switch to the HSICLK. If an interrupt is enabled, the software can receive the related interrupt.

4.5.4 Bus clock

AHB, APB1 and APB2 buses are built in. The clock source of AHB is SYSCLK, and the clock source of APB1 and APB2 is HCLK. The required clock can be obtained by configuring the frequency division factor. The maximum frequency of AHB is 240MHz, the maximum frequency of APB2 is 120MHz, and the maximum frequency of APB1 is 60MHz.

4.5.5 Phase locked loop

The APM32F425xG_F427xG series feature a Phase-Locked Loop (PLL1), which requires configuration parameters to generate different clock frequencies. For the specific parameters and configuration registers, refer to the corresponding user manual.

4.6 Reset and power management

4.6.1 Power supply scheme

Table 14 Power Supply Scheme

Name	Voltage range	Description
V_{DD}	1.8~3.6V	I/O (see pin distribution diagram for specific I/O) and internal voltage regulator are powered through VDD pin.
V_{DDA}/V_{SSA}	1.8~3.6V	Power supply provided for ADC, DAC, reset module, RC oscillator and PLL analog part. When ADC or DAC is used, VDDA and VSSA pins must be connected to V_{DD} and V_{SS}.
V_{BAT}	1.65~3.6V	When V_{DD} is disabled, RTC, external 32kHz oscillator and backup register are powered through internal power switch.

4.6.2 Voltage regulator

Table 15 Regulator Operating Mode(1)

Name	Description
Master mode (MR)	Used in run mode
Low-power mode (LPR)	Used in stop mode
Power-down mode	Used in standby mode. When the voltage regulator has high-impedance output, the core circuit is powered down. The power consumption of the voltage regulator is zero, and all data of registers and SRAM will be lost.

Note: (1) The voltage regulator keeps in working state after reset, and outputs with high impedance in power-down mode.

4.6.3 Power supply voltage monitor

Power-on reset (POR), power-down reset (PDR) and brown-out reset (BOR) circuits are integrated inside the product. These three circuits are always in working condition. When the power-down reset circuit monitors that the power supply voltage is lower than the specified threshold value ($V_{POR/PDR}$), even if the external reset circuit is used, the system will remain reset.

The product has a built-in programmable power supply voltage monitor (PVD) that can monitor V_{DD} and compare it with V_{PVD} threshold. When V_{DD} is outside the V_{PVD} threshold range and the interrupt is enabled, the MCU can be set to a safe state through the interrupt service program.

4.7 Low-power mode

APM32F425xG_F427xG supports three low-power modes which are sleep mode, stop mode and standby mode. There are differences in power, wake-up time and wake-up mode among these three modes. The low-power mode can be selected according to the actual requirements.

Table 16 Low-power Modes

Mode	Description
Sleep mode	● The core stops working. All peripherals are working. Can be woken up through interrupts/events.
Stop mode	● Under the condition that SRAM and register data are not lost, the lowest power consumption can be achieved in stop mode. ● The clock of the internal 1.2V power supply module will stop. HSECLK crystal resonator, HSICLK and PLL will be disabled, and the voltage regulator can be configured in normal mode or low-power mode. ● Any external interrupt line can wake up MCU, and the external interrupt lines include one of the 16 external interrupt lines, PVD output, RTC and USB_OTG.
Standby mode	● The power consumption in this mode is the lowest. ● Internal voltage regulator is turned off. All 1.2V power supply modules are powered down. HSECLK crystal resonator, and HSICLK clocks are disabled. SRAM and register data disappear. RTC area and backup register data remain preserved, and the standby circuit still works.

Mode	Description
	● The external reset signal on NRST, IWDT reset, rising edge on WKUP pin or RTC event will wake MCU to exit standby mode.

4.8 DMA

2 built-in DMA, 16 data streams in total. Each data stream corresponds to 8 channels, but each data stream can only use 1 channel at the same time. The peripherals supporting DMA requests are ADC, DAC, SPI, USART, I2C, SDIO and TMRx. Four levels of DMA channel priority can be configured. Support "memory→memory, memory→peripheral, peripheral→memory" data transmission (the memory includes Flash、SRAM、SDRAM).

4.9 GPIO

GPIO can be configured as general input, general output, multiplexing function and analog input and output. The general input can be configured as floating input, pull-up input and pull-down input. The general output can be configured as push-pull output and open-drain output. The multiplexing function can be used for digital peripherals, and the analog input and output can be used for analog peripherals and low-power mode. The enable and disable pull-up/pull-down resistor can be configured. Different speed can be configured. The higher the speed is, the greater the power and the noise will be.

4.10 Communication peripherals

4.10.1 USART/UART

Up to 6 universal synchronous/asynchronous transmitter receivers are built in the chip. The USART1/6 interfaces can communicate at a rate of 10.5Mbit/s, while other USART/UART interfaces can communicate at a rate of 5.25Mbit/s. All USART/UART interfaces can configure baud rate, parity check bit, stop bit, and data bit length, and they all can support DMA. USART/UART function differences are shown in the table below:

Table 17 USART/UART Function Differences

USART mode/function	USART1	USART2	USART3	UART4	UART5	USART6
Hardware flow control of modem	√	√	√	—	—	√
Smart card mode	√	√	√	—	—	√
IrDA SIR coder-encoder functions	√	√	√	√	√	√
LIN mode	√	√	√	√	√	√
Standard characteristics	√	√	√	√	√	√
SPI host	√	√	√	—	—	√
Maximum baud rate under 16 times oversampling (Mbit/s)	7.5	3.75	3.75	3.75	3.75	7.5

USART mode/function	USART1	USART2	USART3	UART4	UART5	USART6
Maximum baud rate under 8 times oversampling (Mbit/s)	15	7.5	7.5	7.5	7.5	15
APB mapping	APB2	APB1	APB1	APB1	APB1	APB2

Note: √ = support.

4.10.2 I2C

I2C1/2/3 bus interfaces are built-in and they all can work in multiple-master or slave modes, support 7-bit or 10-bit addressing, and support dual-slave addressing in 7-bit slave mode. The communication rate supports standard mode (up to 100kbit/s) and fast mode (up to 400kbit/s). It has a built-in hardware CRC generator and checker that supports DMA operations and is compatible with SMBus 2.0 and PMBus.

4.10.3 SPI

3 built-in SPI, support full-duplex and half-duplex communication in master mode and slave mode. Can use DMA controller, and can configure 4~16 bits per frame. The three SPIs can communicate at maximum rates of 60Mbit/s, 30Mbit/s, and 30Mbit/s respectively.

4.10.4 QSPI

1 built-in QSPI, dedicated for communication, supports DMA operations. It can connect to external Flash memory via single, dual, or quad SPI modes, supporting 8-bit, 16-bit, and 32-bit accesses. Internally, it has an 8-byte transmit FIFO and an 8-byte receive FIFO.

4.10.5 CAN

2 built-in CAN, compatible with 2.0A and 2.0B (active) specifications, and can communicate at a rate of up to 1Mbit/s. It can receive and transmit standard frame of 11-bit identifier and extended frame of 29-bit identifier. It has 3 sending mailboxes, 2 receiving FIFO, along with 14 third-level adjustable filters.

4.10.6 USB_OTG

2 USB OTG_FS controllers, both capable of supporting both host and device functionalities simultaneously, compliant with the USB 2.0 On-The-Go (OTG) standard. They can also be configured in "host-only" or "device-only" modes, fully adhering to the USB 2.0 specifications. The OTG_FS clock (48MHz) is generated by a dedicated PLL output.

4.10.7 Ethernet

Provides an IEEE-802.3-2002 compatible MAC for Ethernet LAN communication over MII or RMII. This MCU requires a PHY connection to a physical LAN bus. The PHY connects to the MII port, uses 17 signals for MII or 9 signals for RMII, and can use a 25MHz clock (MII) from the core.

4.10.8 SDIO

The secure digital input/output interface can connect to SD card, SD I/O card, multi-media card

(MMC) and CE-ATA card master interfaces, and provide data transmission between AHB system bus and SD memory card, SD I/O card, MMC and CE-ATA devices.

4.11 Analog peripherals

4.11.1 ADC

3 built-in ADC with a resolution of 12 bits (configurable to 10 bits, 8 bits, or 6 bits). Each ADC supports up to 16 external channels and 3 internal channels. The internal channels measure the temperature sensor voltage, reference voltage and backup voltage respectively. A/D conversion mode of each channel has single, continuous, scan or intermittent modes. ADC conversion results can be left-aligned or right-aligned and stored in 16-bit data register. Analog watchdog and DMA are also supported.

4.11.1.1 Temperature sensor

1 built-in temperature sensor (TSensor), which is internally connected with ADC_IN16 channel. The voltage generated by the sensor varies linearly with temperature, and the converted voltage value obtained through the ADC can be used to calculate the temperature.

Supported temperature range: -40°C to 125°C.

Table 18 Calibration Value of Temperature Sensor

Calibration Name	Description	Memory Address
V_{sensor_CAL1}	Raw data collected at a temperature of 30°C and V_{DDA} = 3.3V	0x1FFF 7A2C - 0x1FFF 7A2D
V_{sensor_CAL2}	Raw data collected at a temperature of 110°C and V_{DDA} = 3.3V	0x1FFF 7A2E - 0x1FFF 7A2F

4.11.1.2 Internal reference voltage

Built-in reference voltage V_{REFINT}, internally connected to ADC_IN17 channel. V_{REFINT} can be obtained through ADC. V_{REFINT} provides stable voltage output for ADC.

Table 19 Calibration Value of Internal Reference Voltage

Calibration Name	Description	Memory Address
V_{REFINT_CAL}	Raw data collected at a temperature of 25°C (±5°C) and V_{DDA} = 3.3V (±10mV)	0x1FFF 7A2A - 0x1FFF 7A2B

4.11.2 DAC

2 built-in 12-bit DAC, each corresponding to an output channel, which can be configured as 8-bit and 12-bit modes. The DMA function is supported. The waveform generation supports noise wave and triangle wave. The conversion mode supports independent or simultaneous conversion. The trigger mode supports external signal trigger and internal timer update trigger.

4.12 Timer

Two built-in 16-bit advanced timers (TMR1/8), six 16-bit general-purpose timers (TMR9/10/11/12/13/14), four 32-bit general timers (TMR2/3/4/5), two 16-bit basic timers

(TMR6/7), one independent watchdog timer, one window watchdog timer and one system tick timer.

Watchdog timer can be used to detect whether the program is running normally.

The system tick timer is the peripheral which has an auto-reload feature. When the counter reaches zero, it can generate a maskable system interrupt, making it suitable for real-time operating systems and general delays.

Table 20 Function Comparison between Advanced/General-purpose/Basic and System Tick Timers

Timer type	**System tick timer**	**Basic timer**	**General-purpose timer**		**Advanced timer**
Timer name	Sys Tick Timer	TMR6/7	TMR2/3/4/5	TMR9/10/11/12/13/14	TMR1/8
Counter resolution	24 bits	16 bits	32 bits	16 bits	16 bits
Counter type	Down	Up	Up, down, up/down	Up	Up, down, up/down
Prescaler factor	-	Any integer between 1 and 65536	Any integer between 1 and 65536		Any integer between 1 and 65536
Generate DMA request	-	Yes	Yes	No	Yes
Capture/compare register	-	-	4	2 (TMR9/12) 1 (Others)	4
Complementary output	-	No	No		Yes
Pin characteristics	-	-	1-way external trigger signal input pin. 4-way non-complementary channel pin.	2 non-complementary channel pins (TMR9/12), and one other pin.	1-way external trigger signal input pin. 1-way braking input signal pin. 3-pair complementary channel pins. 1-way non-complementary channel pin.
Function Description	Special for real-time operating system. Automatic reloading function supported. When the counter is 0, it	Used to generate DAC trigger signals. Can be used as a 16-bit general-purpose time-based counter.	Synchronization or event linking function is provided. Timers in debug mode can be frozen.	Provides synchronization or event linking functions. In debug mode, the counter can be frozen.	It has complementary PWM output with deadband insertion. When configured as a 16-bit standard timer, it has the same function as the TMRx timer. When configured as a 16-bit PWM generator, it

Timer type	System tick timer	Basic timer	General-purpose timer		Advanced timer
	can generate a maskable system interrupt. Can program the clock source.		Can be used to generate PWM output. Each timer has independent DMA request mechanism. Can handle incremental encoder signals.	Can be used to generate PWM output. Capable of handling signals from incremental encoders.	has full modulation capability (0~100%). In debug mode, the timer can be frozen, and PWM output is disabled. Synchronization or event linking function is provided.

Table 21 Function Comparison between IWDT and WWDT

Name	Counter resolution	Counter type	Prescaler factor	Function description
Independent watchdog	12 bits	Down	Any integer between 1 and 256	The clock is provided by an internally independent RC oscillator of 28kHz, which is independent of the master clock, so it can run in stop and standby modes. The entire system can be reset in case of problems. It can provide timeout management for applications as a free-running timer. It can be configured as a software or hardware startup watchdog through option bytes. Timers in debug mode can be frozen.
Window watchdog	7 bits	Down	-	Can be set for free running. The entire system can be reset in case of problems. Driven by the master clock, it has early interrupt warning function. Timers in debug mode can be frozen.

4.13 RTC

1 RTC is built in. There are LSECLK signal input pins (OS32_IN and OS32_OUT) and 1 TAMP input signal detection pins (RTC_TAMP1). The clock source can be selected from external 32.768kHz crystal oscillator, resonator or oscillator, LSICLK and HSECLK/128. It is powered by V_{DD} by default. When V_{DD} is powered off, it can be automatically switched to V_{BAT} power supply, and RTC configuration and time data will not be lost. RTC configuration and time data will not be lost in case of system reset, software reset or power-on reset. It supports clock and calendar functions.

4.13.1 Backup domain

4KB backup SRAM and 20 backup registers are built in. They are powered by V_{DD} by default. When V_{DD} is powered off, it can be automatically switched to V_{BAT} power supply, and the data in backup register will not be lost. The data in backup register will not be lost in case of system reset, software reset or power-on reset.

4.14 RNG

A build-in RNG provides 32-bit random values generated by the integrated analog source.

4.15 CRC

1 CRC (Cyclic Redundancy Check) computing unit is built in, which can generate CRC codes and handle 8-bit, 16-bit and 32-bit data.

5 Electrical Characteristics

5.1 Test conditions of electrical characteristics

5.1.1 Maximum and minimum values

Unless otherwise specified, all products are tested on the production line at T_A=25℃. Its maximum and minimum values can support the worst environmental temperature, power supply voltage and clock frequency.

In the notes at the bottom of each table, it is stated that the data are obtained through comprehensive evaluation, design simulation or process characteristics and are not tested on the production line. On the basis of comprehensive evaluation, after passing the sample test, take the average value and add and subtract three times the standard deviation (average ±3∑) to get the maximum and minimum values.

5.1.2 Typical value

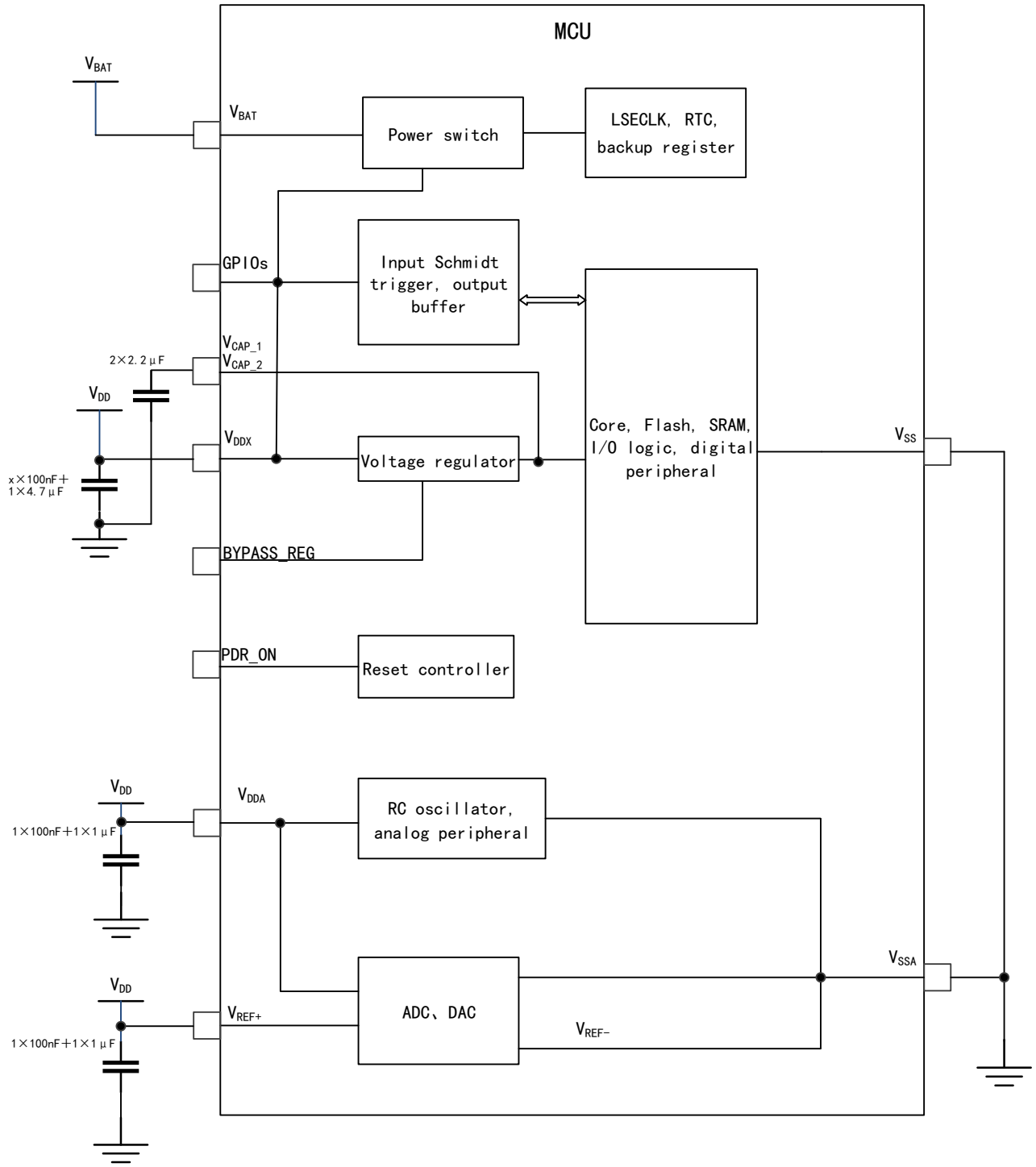
Unless otherwise specified, typical data are measured based on T_A=25℃, V_{DD}=V_{DDA}=3.3V. These data are only used for design guidance.

5.1.3 Typical curve

Unless otherwise specified, typical curves are only used for design guidance and are not tested.

5.1.4 Power supply scheme

Figure 8 Power Supply Scheme



Notes: V_{DDx} in the figure means the number of V_{DD} is x.

5.1.5 Load capacitance

Figure 9 Load conditions when measuring pin parameters

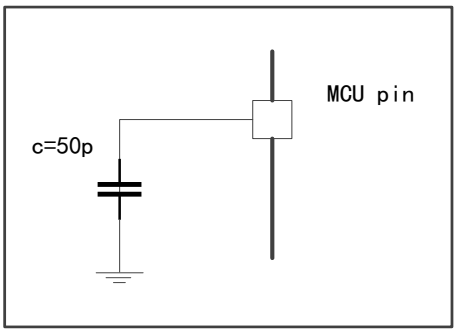


Figure 10 Pin Input Voltage Measurement Scheme

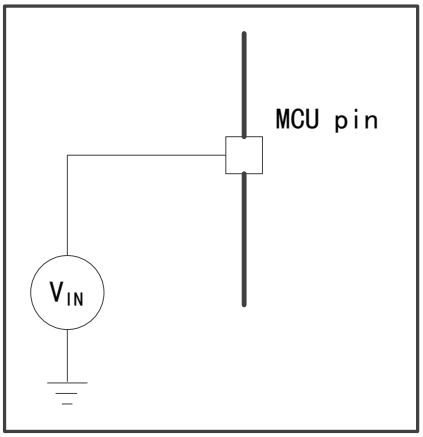
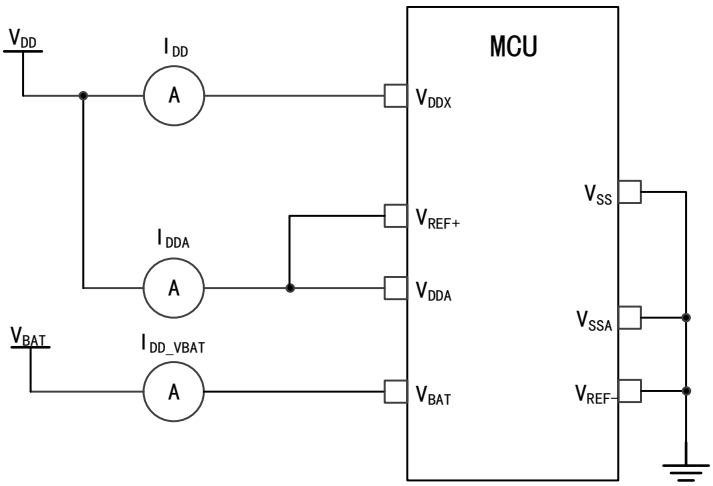


Figure 11 Power Consumption Measurement Scheme



5.2 Test under general operating conditions

Table 22 General Operating Conditions

Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
f_{HCLK}	Internal AHB clock frequency	-	-	240	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	-	60	
f_{PCLK2}	Internal APB2 clock frequency	-	-	120	
V_{DD}	Main power supply voltage	-	1.8	3.6	V
V_{DDA}	Analog power supply voltage (When neither ADC nor DAC is used)	Must be the same as V_{DD}	1.8	2.4	V
	Analog power supply voltage (When ADC and DAC are used)		2.4	3.6	
V_{BAT}	Power supply voltage of backup domain	-	1.65	3.6	V
T_A	Ambient temperature (temperature number 6)	Maximum power dissipation	-40	85	℃
	Ambient temperature (temperature number 7)		-40	105	

Table 23 Chip startup time

Symbol	Description	Conditions	Minimum value	Typical value	Maximum value	Unit
$T_{start-up}$	Chip startup time	-	8	9	10	ms

5.3 Absolute maximum ratings

If the load on the device exceeds the absolute maximum rating, it may cause permanent damage to the device. Only the maximum load that can be borne is provided, and there is no guarantee that the device operates normally under this condition.

5.3.1 Maximum temperature characteristics

Table 24 Temperature Characteristics

Symbol	Description	Value	Unit
T_{STG}	Storage temperature range	-65 ~ +150	°C
T_J	Maximum junction temperature	125	

5.3.2 Maximum rated voltage characteristics

All power supply (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the power supply within the external limited range.

Table 25 Maximum Rated Voltage Characteristics

Symbol	Description	Minimum value	Maximum value	Unit
V_{DD} - V_{SS}	External main power supply voltage	-0.3	4.0	V
V_{IN}	Input voltage on 5V tolerant pins	V_{SS}-0.3	V_{DD}+4	
	Input voltage on other pins	V_{SS}-0.3	4.0	
$\lvert \Delta V_{DDx} \rvert$	Voltage difference between different power supply pins	-	50	mV
$\lvert V_{SSx}-V_{SS} \rvert$	Voltage difference between different grounding pins	-	50	

5.3.3 Maximum rated current characteristics

Table 26 Current Characteristics

Symbol	Description	Maximum value	Unit
I_{VDD}	Total current through V_{DD}/V_{DDA} power line (supply current) (1)	240	mA
I_{VSS}	Total current through V_{SS} ground line (outflow current) (1)	240	
I_{IO}	Sink current on any I/O and control pin	25	
	Source current on any I/O and control pin	25	
$I_{INJ(PIN)}$ (2)	Injection current of 5T pin(3)	-5/+0	
	Injection current of other pins(4)	±5	
$\Sigma I_{INJ(PIN)}$(2)	Total injection current on all I/O and control pins (5)	±25	

Note:

(1) All power supply (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) must always be within the allowed range.

(2) The outflow current will interfere with the analog performance of the device.

(3) I/O cannot be injected positively: when $V_{IN}<V_{SS}$, $I_{INJ(PIN)}$ cannot exceed the maximum allowed input current.

(4) If V_{IN} exceeds the maximum value, $I_{INJ(PIN)}$ must be externally limited not to exceed the maximum value. When $V_{IN}> V_{DD}$, the current flows into the pins; when $V_{IN}<V_{SS}$, the current flows out of the pins.

(5) When the current is injected into several I/O ports at the same time, the maximum value of $\Sigma I_{INJ(PIN)}$ is the sum of the absolute values of the instantaneous inflow current and outflow current.

5.3.4 Electrostatic discharge (ESD)

Table 27 ESD Absolute Maximum Ratings(1)

Symbol	Parameter	Conditions	Range	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human body model)	TA=+25℃, conforming to ANSI/ESDA/JEDEC JS-001-2017	±4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charged device model)	TA=+25℃, conforming to ANSI/ESDA/JEDEC JS-002-2018	±1000	

Note: (1) The samples are measured by a third-party testing organization and are not tested in production.

5.3.5 Static latch-up (LU)

Table 28 Static Latch-up(1)

Symbol	Parameter	Conditions	Type
LU	Class of static latch-up	T_A=+105℃, conforming to JEDEC JESD78F-2022	Class II A

Note: (1) The samples are measured by a third-party testing organization and are not tested in production.

5.4 On-chip memory

5.4.1 Flash characteristics

Table 29 Flash Memory Characteristics(1)

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
t_{prog}	8/16/32-bit programming time	T_A = -40~105℃ V_{DD}=2.4~3.6V	-	43	60	μs
t_{ERASE1}	Page (16KBytes) erase time	T_A = -40~105℃ V_{DD}=2.4~3.6V	-	60	120	ms
t_{ERASE2}	Page (64KBytes) erase time		-	250	500	
t_{ERASE3}	Page (128KBytes) erase time		-	500	1000	
t_{ME}	Mass erase time	T_A = -40~105℃ V_{DD}=2.4~3.6V	-	10	20	ms
V_{prog}	Voltage of 8-bit programming	T_A = -40~105℃	1.8	-	3.6	V
	Voltage of 16-bit programming		2.1	-	3.6	
	Voltage of 32-bit/64-bit programming		2.7	-	3.6	

Note: (1) The data are obtained from a comprehensive evaluation and are not tested in production.

Table 30 Flash Memory Lifespan and Data Retention Time(1)

Symbol	Parameter	Conditions	Minimum value	Unit
N_{END}	Lifespan (number of write/erase cycles)	T_A=–40~105℃	100	kcycles
t_{RET}	Data retention	10 kcycles, T_A=125℃	10	Years

Note: (1) The data are obtained from a comprehensive evaluation and are not tested in production.

5.5 EMC

5.5.1 Electromagnetic Compatibility (EMC)

Table 31 EMC

Symbol	Parameter	Conditions	Type
V_{ESD}	The voltage applied to all device pins causes malfunctions.	V_{DD}=3.3V, T_A=25℃ LQFP144, f_{HCLK}=240MHz Conforming to IEC 61000-4-2	3A

Symbol	Parameter	Conditions	Type
V_{EFT}	Rapid transient voltage spikes induce malfunctions. VDD and VSS pins with 100pF.	V_{DD}=3.3V, T_A=25℃ LQFP144, f_{HCLK}=240MHz Conforming to IEC 61000-4-4	

5.5.2 Electromagnetic Interference (EMI)

Table 32 EMI

Symbol	Parameter	Conditions	Test frequency	Maxvs. [f_{HXTAL}/f_{HCLK}] 25/240 MHz	Unit
S_{EMI}	Peak Detection	V_{DD}=3.6V, T_A=+25°C LQFP144, f_{HCLK}=240MHz Conforming to SAE J1752-3:2017	0.15MHz to 30MHz	3.60	dBμV
			30MHz to 130MHz	12.09	
			130MHz to 1GHz	8.59	

5.6 Clock

5.6.1 Characteristics of external clock source

5.6.1.1 High-speed external clock generated by crystal resonator

For detailed parameters (frequency, package, precision, and so on) of crystal resonator, consult the corresponding manufacturer.

Table 33 HSECLK 4~26MHz Oscillator Characteristics(1)

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	26	MHz
R_F	Feedback resistance	-	-	200	-	kΩ
$t_{SU(HSECLK)}$(2)	Start-up time	V_{DD} is stable	-	-	9	ms
G_m	Oscillator transconductance	Enable	5.65	-	-	mA/V

Note:

(1) The data are obtained from a comprehensive evaluation and are not tested in production.

(2) The HSECLK startup time is related to the characteristics of the crystal oscillator.

5.6.1.2 Low-speed external clock generated by crystal resonator

For detailed parameters (frequency, package, precision, and so on) of crystal resonator, consult the corresponding manufacturer.

Table 34 LSECLK Oscillator Characteristics (f_{LSECLK} =32.768kHz)(1)

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
f_{OSC_IN}	Oscillator frequency	-	-	32.768	-	kHz

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
$I_{DD(LSECLK)}$	LSECLK current consumption	-	-	-	1	μA
$t_{SU(LSECLK)}$(2)	Start-up time	V_{DD} is stable	-	2	-	s

Note:

(1) The data are obtained from a comprehensive evaluation and are not tested in production.

(2) $t_{SU(LSECLK)}$ is the startup time, which is measured from the time when LSECLK is enabled by software to the time when stable oscillation at 32.768kHz is obtained. This value is measured by using a standard crystal resonator, which may vary due to different crystal manufacturers.

5.6.2 Characteristics of internal clock source

5.6.2.1 High-speed internal (HSICLK) RC oscillator

Table 35 HSICLK Oscillator Characteristics(1)

Symbol	Parameter	Conditions		Minimum value	Typical value	Maximum value	Unit
f_{HSICLK}	Frequency	-		-	16	-	MHz
$A_{CC(HSICLK)}$	Accuracy of HSICLK oscillator	Factory calibration	V_{DD}=3.3V，T_A=25℃	-1	-	1	%
			V_{DD}=2-3.6V，T_A=-40~105℃	-2	-	4	%
$I_{DDA(HSICLK)}$	Power consumption of HSICLK oscillator	-		-	100	120	μA
$t_{SU(HSICLK)}$	Startup time of HSICLK oscillator	V_{DD}=3.3V，T_A=-40~105℃		-	3.7	5	μs

Note: (1) The data are obtained from a comprehensive evaluation and are not tested in production.

5.6.2.2 Low-speed internal (LSICLK) RC oscillator

Table 36 LSICLK Oscillator Characteristics(1)

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
f_{LSICLK}	Frequency (V_{DD}=2-3.6V, T_A =-40~105℃)	20	32	40	kHz
$I_{DD(LSICLK)}$	Power consumption of LSICLK oscillator	-	0.4	0.6	μA
$t_{SU(LSICLK)}$	Startup time of LSICLK oscillator (V_{DD}=3.3V，T_A=-40~105℃)	-	16	40	μs

Note: (1) The data are obtained from a comprehensive evaluation and are not tested in production.

5.6.3 PLL characteristics

Table 37 PLL1 Characteristics(1)

Symbol	Parameter	Value			Unit
		Minimum value	Typical value	Maximum value	
f_{PLL1_IN}	PLL1 input clock	0.92	1	2.1	MHz
	PLL1 input clock duty cycle	40	-	60	%
f_{PLL1_OUT}	PLL1 frequency multiplier output clock (V_{DD}=3.3V, T_A=-40~105℃)	24	-	240	MHz
$f_{PLL1\_48\_OUT}$	PLL1 frequency multiplier output 48MHz clock (V_{DD}=3.3V, T_A=-40~105℃)	-	48	75	MHz
t_{LOCK1}	PLL1 phase locking time	60	-	120	μs

Note: (1) The data are obtained from a comprehensive evaluation and are not tested in production.

5.7 Reset and power management

5.7.1 Power-on/power-down characteristics

Table 38 Power-on/power-down Characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
t_{VDD}	V_{DD} rise time rate	-	10	-	200000	μs/V
	V_{DD} fall time rate		10	-	200000	

5.7.2 Test of embedded reset and power control module characteristics

Table 39 Embedded Reset and Power Control Module Characteristics(1)

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
$V_{POR/PDR}$	Power-on/power-down reset threshold	Falling edge	1.68	1.70	1.70	V
		Rising edge	1.71	1.72	1.73	
V_{BOR1}	Brown-out reset threshold level 1	Falling edge	2.19	2.21	2.24	
		Rising edge	2.27	2.29	2.30	
V_{BOR2}	Brown-out reset threshold level 2	Falling edge	2.49	2.51	2.55	
		Rising edge	2.56	2.58	2.59	
V_{BOR3}	Brown-out reset threshold level 3	Falling edge	2.81	2.84	2.87	
		Rising edge	2.89	2.91	2.92	
$V_{BORhyst}$	BOR hysteresis	-	-	100	-	mV
$V_{PDRhyst}$	PDR hysteresis	-	-	40.00	50.00	
$T_{RSTTEMPO}$	Reset duration	-	0.70	0.95	1.48	ms

Note: (1) The data are obtained from a comprehensive evaluation and are not tested in production.

Table 40 Programmable Power Supply Voltage Detector Characteristics(1)

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
V_{PVD}	Programmable power supply voltage detector voltage level selection	PLS[2:0]=000 (rising edge)	2.14	-	2.18	V
		PLS[2:0]=000 (falling edge)	2.03	-	2.10	V
		PLS[2:0]=000 (PVD hysteresis)	80.00	-	120.00	mV
		PLS[2:0]=001 (rising edge)	2.30	-	2.34	V
		PLS[2:0]=001 (falling edge)	2.18	-	2.23	V
		PLS[2:0]=001 (PVD hysteresis)	90.00	-	120.00	mV
		PLS[2:0]=010 (rising edge)	2.44	-	2.48	V
		PLS[2:0]=010 (falling edge)	2.32	-	2.37	V
		PLS[2:0]=010 (PVD hysteresis)	110	-	120	mV
		PLS[2:0]=011 (rising edge)	2.58	-	2.63	V
		PLS[2:0]=011 (falling edge)	2.49	-	2.53	V
		PLS[2:0]=011 (PVD hysteresis)	90	-	100	mV
		PLS[2:0]=100 (rising edge)	2.75	-	2.80	V
		PLS[2:0]=100 (falling edge)	2.64	-	2.68	V
		PLS[2:0]=100 (PVD hysteresis)	110	-	120	mV
		PLS[2:0]=101 (rising edge)	2.91	-	2.97	V
		PLS[2:0]=101 (falling edge)	2.81	-	2.86	V
		PLS[2:0]=101 (PVD hysteresis)	100	-	110	mV
		PLS[2:0]=110 (rising edge)	3.02	-	3.08	V
		PLS[2:0]=110 (falling edge)	2.90	-	2.96	V
		PLS[2:0]=110 (PVD hysteresis)	110	-	120	m.V
		PLS[2:0]=111 (rising edge)	3.12	-	3.19	V
		PLS[2:0]=111 (falling edge)	3.00	-	3.07	V
		PLS[2:0]=111 (PVD hysteresis)	110	-	120	mV

Note: (1) The data are obtained from a comprehensive evaluation and are not tested in production.

5.8 Power consumption

5.8.1 Power consumption test environment

（1） The values are measured by executing Dhrystone 2.1, with the Keil.V5 compilation environment and the L0 compilation optimization level.

（2） All I/O pins are in analog input mode and are connected to a static level at V_{DD} or V_{SS} (no load).

（3） Unless otherwise specified, all peripherals are disabled.

（4） The relationship between Flash wait cycle setting and f_{HCLK}:

- 0~30MHz: 0 wait cycle
- 30~60MHz: 1 wait cycle
- 60~90MHz: 2 wait cycles
- 90~120MHz: 3 wait cycles
- 120~150MHz: 4 wait cycles
- 150~180MHz：5 wait cycles
- 180~210MHz：6 wait cycles
- 210~240MHz：7 wait cycles

（5） When the peripherals are enabled: $f_{PCLK1}=f_{HCLK}/4$, $f_{PCLK2}=f_{HCLK}/2$

5.8.2 Power consumption in run mode

Table 41 Power Consumption in Run Mode When the Program is Executed in Flash (FACC is turned on)

Parameter	Conditions	f_{HCLK}	Typical value (1)		Maximum value (1)	
			T_A=25℃，V_{DD}=3.3V		T_A=105℃，V_{DD}=3.6V	
			I_{DDA}(μA)	I_{DD}(mA）	I_{DDA}(μA)	I_{DD}(mA)
Power consumption in run mode	HSECLK bypass (2), enabling all peripherals (3)	240MHz	1000	72.5	1000	84
		210MHz	900	70.5	920	80
		180MHz	820	69	840	76
		168MHz	751.56	67.70	802.2	74.02
		144MHz	693.94	52.75	745.2	57.66
		120MHz	637.4	44.49	691.1	49.39
		90MHz	780.88	34.37	831.7	39.375
		60MHz	636.86	23.86	689.6	28.7
		30MHz	636.62	13.29	689.4	18.099
		25MHz	115.372	10.83	127.76	15.627
		16MHz	115.418	7.21	127.93	11.905
		8MHz	115.36	3.93	127.77	8.587
		4MHz	115.328	2.31	127.78	6.967
		2MHz	115.36	1.49	127.82	6.17
	HSECLK bypass (2), disabling all peripherals	240MHz	1000	43.1	1000	54
		210MHz	900	38	920	48
		180MHz	820	32	840	40
		168MHz	750.88	28.35	801.4	34.352
		144MHz	692.84	22.02	744.7	26.958
		120MHz	636.82	18.54	691.1	23.48

Parameter	Conditions	f_{HCLK}	Typical value (1)		Maximum value (1)	
			T_A=25℃，V_{DD}=3.3V		T_A=105℃，V_{DD}=3.6V	
			I_{DDA}(μA)	I_{DD}(mA）	I_{DDA}(μA)	I_{DD}(mA)
		90MHz	779.8	14.45	831.9	19.302
		60MHz	636.52	10.04	689.8	14.924
		30MHz	636.4	5.75	690.2	10.563
		25MHz	115.318	4.38	128.66	9.115
		16MHz	115.344	3.01	128.44	7.673
		8MHz	115.358	1.86	127.8	6.481
		4MHz	115.348	1.27	127.84	5.93
		2MHz	115.36	0.99	127.86	5.645

Note:

(1) The data are obtained from a comprehensive evaluation and are not tested in production.

(2) The external clock is 4MHz. When f_{HCLK}>25MHz, turn on PLL; otherwise, turn off PLL.

(3) When the analog peripherals such as ADC, DAC, HSECLK, LSECLK, HSICLK and LSICLK are turned on, extra power consideration needs to be considered.

Table 42 Power Consumption in Run Mode when the Program is Executed in Flash (FACC is turned off)

Parameter	Conditions	f_{HCLK}	Typical value (1)		Maximum value (1)	
			T_A=25℃，V_{DD}=3.3V		T_A=105℃，V_{DD}=3.6V	
			I_{DDA}(μA)	I_{DD}(mA）	I_{DDA}(μA)	I_{DD}(mA)
Power consumption in run mode	HSECLK bypass (2), enabling all peripherals (3)	240MHz	1000	69.5	1000	81
		210MHz	900	67.6	920	77
		180MHz	820	66	840	73
		168MHz	751.66	64.25	802	70.52
		144MHz	693.58	51.09	745.3	56.05
		120MHz	637.26	43.99	690.2	48.92
		90MHz	780.86	34.91	831.4	39.971
		60MHz	636.78	25.02	689.4	29.894
		30MHz	636.66	14.33	689	19.315
		25MHz	115.362	11.80	127.72	16.725
		16MHz	115.362	7.83	127.75	12.527
		8MHz	115.35	4.27	127.8	8.994
		4MHz	115.35	2.45	127.88	7.13
		2MHz	115.362	1.57	127.76	6.279
		240MHz	1000	40.1	1000	51

Parameter	Conditions	f_{HCLK}	Typical value (1)		Maximum value (1)	
			T_A=25℃，V_{DD}=3.3V		T_A=105℃，V_{DD}=3.6V	
			I_{DDA}(μA)	I_{DD}(mA）	I_{DDA}(μA)	I_{DD}(mA)
	HSECLK bypass (2), disabling all peripherals	210MHz	900	35	920	45
		180MHz	820	29	840	37
		168MHz	750.94	24.71	801.4	30.851
		144MHz	692.82	20.21	744.7	25.179
		120MHz	636.76	17.96	689.8	22.905
		90MHz	780.46	15.03	831.6	20.009
		60MHz	636.46	11.19	689.8	16.127
		30MHz	636.38	6.79	689.9	11.675
		25MHz	115.33	5.26	128.5	10.148
		16MHz	115.32	3.65	127.96	8.458
		8MHz	115.364	2.14	127.82	6.8
		4MHz	115.35	1.43	127.68	6.114
		2MHz	115.532	1.07	127.9	5.815

Note:

(1) The data are obtained from a comprehensive evaluation and are not tested in production.

(2) The external clock is 4MHz. When f_{HCLK}>25MHz, turn on PLL; otherwise, turn off PLL.

(3) When the analog peripherals such as ADC, DAC, HSECLK, LSECLK, HSICLK and LSICLK are turned on, extra power consideration needs to be considered.

Table 43 Power Consumption in Run Mode when the Program is Executed in RAM

Parameter	Conditions	f_{HCLK}	Typical value (1)		Maximum value (1)	
			T_A=25℃，V_{DD}=3.3V		T_A=105℃，V_{DD}=3.6V	
			I_{DDA}(μA)	I_{DD}(mA)	I_{DDA}(μA)	I_{DD}(mA)
Power consumption in run mode	HSECLK bypass (2), enabling all peripherals (3)	240MHz	1000	77.7	1000	89
		210MHz	900	74	920	84
		180MHz	820	72	840	80
		168MHz	752.14	70.29	803.8	76.51
		144MHz	693.74	54.73	745.5	59.73
		120MHz	637.6	46.22	690.4	51.16
		90MHz	781	35.67	832	40.53
		60MHz	637.02	24.70	689.8	29.646
		30MHz	636.74	13.74	689.2	18.596
		25MHz	115.42	11.23	127.85	16.02

Parameter	Conditions	f_{HCLK}	Typical value (1)		Maximum value (1)	
			T_A=25℃，V_{DD}=3.3V		T_A=105℃，V_{DD}=3.6V	
			I_{DDA}(μA)	I_{DD}(mA)	I_{DDA}(μA)	I_{DD}(mA)
		16MHz	115.374	7.42	127.88	12.204
		8MHz	115.37	4.05	127.81	8.836
		4MHz	115.376	2.38	127.72	7.124
		2MHz	115.347	1.53	127.76	6.267
	HSECLK bypass (2), disabling all peripherals	240MHz	1000	49.35	1000	59
		210MHz	900	42	920	51
		180MHz	820	36	840	45
		168MHz	751.38	31.03	802.4	37.286
		144MHz	693	24.11	744.7	29.106
		120MHz	636.88	20.30	689.8	25.226
		90MHz	780.56	15.81	931.6	20.743
		60MHz	636.68	10.92	690	15.802
		30MHz	636.62	6.19	689.7	11.021
		25MHz	115.364	4.75	128.42	9.478
		16MHz	115.348	3.26	128.79	8.067
		8MHz	115.378	1.97	127.76	6.706
		4MHz	115.364	1.33	127.73	6.037
		2MHz	115.34	1.02	127.74	5.703

Note:

(1) The data are obtained from a comprehensive evaluation and are not tested in production.

(2) The external clock is 4MHz. When f_{HCLK}>25MHz, turn on PLL; otherwise, turn off PLL.

(3) When the analog peripherals such as ADC, DAC, HSECLK, LSECLK, HSICLK and LSICLK are turned on, extra power consideration needs to be considered.

5.8.3 Power consumption in sleep mode

Table 44 Power Consumption in Sleep Mode when Program is Executed in Flash (FACC is turned off)

Parameter	Conditions	f_{HCLK}	Typical value (1)		Maximum value (1)	
			T_A=25℃，V_{DD}=3.3V		T_A=105℃，V_{DD}=3.6V	
			I_{DDA}(μA)	I_{DD}(mA)	I_{DDA}(μA)	I_{DD}(mA)
Power consumption in sleep mode	HSECLK bypass (2), enabling all peripherals	240MHz	1000	59	1000	71
		210MHz	900	57	920	67
		180MHz	820	55	840	63
		168MHz	751.34	54.18	802.1	60.33

Parameter	Conditions	f_{HCLK}	Typical value (1)		Maximum value (1)	
			T_A=25℃，V_{DD}=3.3V		T_A=105℃，V_{DD}=3.6V	
			I_{DDA}(μA)	I_{DD}(mA)	I_{DDA}(μA)	I_{DD}(mA)
		144MHz	693.26	42.25	745	47.12
		120MHz	637.24	35.75	689.8	40.53
		90MHz	780.6	27.69	831.2	32.539
		60MHz	636.72	19.33	689.2	24.149
		30MHz	636.46	11.02	689.2	15.8
		25MHz	115.356	8.96	127.77	13.7
		16MHz	115.34	5.99	127.71	10.68
		8MHz	115.334	3.33	127.78	8.01
		4MHz	115.332	2.00	127.84	6.669
		2MHz	115.352	1.34	127.82	6.017
	HSECLK bypass (2), disabling all peripherals	240MHz	1000	20.7	1000	31
		210MHz	900	17	920	26
		180MHz	820	15	840	22
		168MHz	750.52	13.91	801	19.858
		144MHz	692.58	10.82	743.9	15.637
		120MHz	636.46	9.20	689	13.987
		90MHz	780.24	7.44	830.6	12.206
		60MHz	636.42	5.33	689	10.067
		30MHz	636.36	3.38	688.8	8.099
		25MHz	115.374	2.41	127.84	7.075
		16MHz	115.346	1.79	127.74	6.459
		8MHz	115.354	1.23	127.83	5.914
		4MHz	115.36	0.96	127.86	5.63
		2MHz	115.422	0.83	127.84	5.535

Note:

(1) The data are obtained from a comprehensive evaluation and are not tested in production.

(2) The external clock is 4MHz; when f_{HCLK}>25MHz, turn on PLL; otherwise, turn off PLL.

5.8.4 Power consumption in stop mode

Table 45 Power Consumption in Stop Mode

Conditions		Typical value (1), (T_A=25℃)			Maximum value (1), (V_{DD}=3.6V)
		V_{DD}=2.4V	V_{DD}=3.3V	V_{DD}=3.6V	T_A=105℃
		I_{DDA}+$I_{DD(mA)}$	I_{DDA}+$I_{DD(mA)}$	I_{DDA}+$I_{DD(mA)}$	I_{DDA}+$I_{DD(mA)}$
The regulator is in run mode, and all oscillators are in off state	Flash is in stop mode, and RC internal oscillator and high-speed oscillator are turned off (with no independent watchdog)	0.5	0.55	0.58	20
	Flash is in power-down mode, and RC internal oscillator and high-speed oscillator are turned off (with no independent watchdog)	0.4	0.45	0.48	20.5
The regulator is in low-power mode, and all oscillators are in off state	Flash is in stop mode, and RC internal oscillator and high-speed oscillator are turned off (with no independent watchdog)	0.3	0.35	0.38	18.5
	Flash is in power-down mode, and RC internal oscillator and high-speed oscillator are turned off (with no independent watchdog)	0.28	0.32	0.35	19

Note: (1) The data are obtained from a comprehensive evaluation and are not tested in production.

5.8.5 Power consumption in standby mode

Table 46 Power Consumption in Standby Mode

Conditions		Typical value (1), (T_A=25℃)						Maximum value (1), (V_{DD}=3.6V)	
		V_{DD}=2.4V		V_{DD}=3.3V		V_{DD}=3.6V		T_A=105℃	
		I_{DDA} (μA)	I_{DD} (μA)	I_{DDA} (μA)	I_{DD} (μA)	I_{DDA} (μA)	I_{DD} (μA)	I_{DDA} (μA)	I_{DD} (μA)
Power supply current in standby mode	The backup SRAM is turned on, and the low-speed oscillator and RTC are turned on	2.15	8.38	2.56	9.73	2.83	10.19	3.76	59.39
	The backup SRAM is turned off, and the low-speed oscillator and RTC are turned on	2.15	3.52	2.62	4.46	2.81	5.11	3.48	32.00

Conditions		Typical value (1), (T_A=25℃)						Maximum value (1), (V_{DD}=3.6V)	
		V_{DD}=2.4V		V_{DD}=3.3V		V_{DD}=3.6V		T_A=105℃	
		I_{DDA} (μA)	I_{DD} (μA)	I_{DDA} (μA)	I_{DD} (μA)	I_{DDA} (μA)	I_{DD} (μA)	I_{DDA} (μA)	I_{DD} (μA)
	The backup SRAM is turned on, and the RTC is turned off	2.13	7.33	2.62	8.24	2.81	8.64	3.45	58.24
	The backup SRAM is turned off, and the RTC is turned off	2.13	2.51	2.61	3.31	2.78	3.68	3.45	19.20

Note: (1) The data are obtained from a comprehensive evaluation and are not tested in production.

5.8.6 Peripheral power consumption

Peripheral power consumption = current that enables the peripheral clock − current that disables the peripheral clock.

Table 47 Peripheral Power Consumption

Parameter	Peripheral	Typical value (1) T_A=25℃, V_{DD}=3.3V			Unit
		240MHz	168MHz	144MHz	
AHB1 (up to 240MHz)	DMA1	7	5.4	4.21	mA
	DMA2	7.5	5.56	4.3	
	ETH	4	3	2.35	
	GPIOA	0.4	0.32	0.25	
	GPIOB	0.4	0.31	0.24	
	GPIOC	0.4	0.32	0.24	
	GPIOD	0.4	0.3	0.23	
	GPIOE	0.4	0.31	0.25	
	GPIOF	0.4	0.33	0.26	
	GPIOG	0.4	0.3	0.24	
	GPIOH	0.4	0.3	0.24	
	CRC	0.04	0.03	0.03	
AHB2 (up to 240MHz)	OTG_FS1	4	3.12	2.41	mA
	OTG_FS2	4	3.12	2.41	
	RNG	0.2	0.16	0.12	
	QSPI	-	-	-	
AHB3 (up to 240MHz)	EMMC	2.2	1.68	1.3	mA
	TMR2	0.6	0.46	0.36	

Parameter	Peripheral	Typical value (1) T_A=25℃, V_{DD}=3.3V			Unit
		240MHz	168MHz	144MHz	
APB1 (up to 60MHz)	TMR3	0.6	0.35	0.27	mA
	TMR4	0.6	0.34	0.27	
	TMR5	0.6	0.46	0.35	
	TMR6	0.2	0.08	0.07	
	TMR7	0.2	0.08	0.06	
	TMR12	0.3	0.19	0.15	
	TMR13	0.3	0.14	0.11	
	TMR14	0.3	0.14	0.1	
	WWDT	0.03	0.02	0.02	
	SPI2	0.2	0.12	0.1	
	SPI3	0.2	0.12	0.1	
	USART2	0.15	0.11	0.09	
	USART3	0.18	0.12	0.09	
	UART4	0.15	0.11	0.08	
	UART5	0.15	0.11	0.08	
	I2C1	0.16	0.12	0.09	
	I2C2	0.16	0.12	0.09	
	I2C3	0.16	0.12	0.1	
	CAN1	0.24	0.18	0.14	
	CAN2	0.24	0.16	0.13	
	PMU	0.01	0.01	0.01	
	DAC	0.12	0.08	0.06	
APB2 (up to 120MHz)	SDIO	0.6	0.41	0.32	
	TMR1	1.2	0.99	0.77	
	TMR8	1.2	0.97	0.77	
	TMR9	0.7	0.41	0.32	
	TMR10	0.4	0.27	0.21	
	TMR11	0.4	0.26	0.22	
	ADC1	0.35	0.27	0.22	
	ADC2	0.35	0.27	0.22	
	ADC3	0.35	0.28	0.23	
	SPI1	0.15	0.12	0.11	

Parameter	Peripheral	Typical value (1) T_A=25℃, V_{DD}=3.3V			Unit
		240MHz	168MHz	144MHz	
	USART1	0.3	0.22	0.18	
	USART6	0.3	0.21	0.18	
	SYSCFG	0.05	0.05	0.05	

Note: (1) The data are obtained from a comprehensive evaluation and are not tested in production.

5.8.7 Backup domain power consumption

Table 48 V_{BAT} Power Consumption

Symbol	Parameter	Conditions	Typical value (1), T_A=25℃		Maximum value (1), V_{BAT}=3.6V		Unit
			V_{BAT}=2.4V	V_{BAT}=3.3V	T_A=85℃	T_A=105℃	
I_{DD_VBAT}	LSECLK and RTC are in ON state	The backup SRAM is turned on, and the low-speed oscillator and RTC are turned on	1.894	2.262	6	11	μA
		The backup SRAM is turned off, and the low-speed oscillator and RTC are turned on	1.08	1.412	3	5	
		The backup SRAM is turned on, and the RTC is turned off	0.926	1.116	5	10	
		The backup SRAM is turned off, and the RTC is turned off	0.02	0.128	2	4	

Note: (1) The data are obtained from a comprehensive evaluation and are not tested in production.

5.9 Wake-up time in low-power mode

The measurement of wake-up time in low-power mode is from the start of wake-up event to the time when the user program reads the first instruction, in which V_{DD}=V_{DDA}.

Table 49 Wake-up Time in Low-power Mode(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{WUSLEEP}$	Wake-up from sleep mode	-	39.00	59	61.20	ns
t_{WUSTOP}	Wake up from the stop mode	The regulator is in run mode, and Flash is in stop state	12.51	13.602	14.99	μs
		The regulator is in low-power mode, and Flash is in stop state	15.51	19.552	22.93	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		The regulator is in run mode, and Flash is in deep power-down mode	125.63	133.156	135.16	
		The regulator is in low-power mode, and Flash is in deep power-down mode	133.52	136.956	139.60	
$t_{WUSTDBY}$	Wake up from standby mode	-	8	9	10	ms

Note: (1) The data are obtained from a comprehensive evaluation and are not tested in production.

5.10 I/O port characteristics

Table 50 DC Characteristics (T_A=-40℃-105℃, V_{DD}=2-3.6V)(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low-level input voltage	5T and 5Tf I/O	-	-	$0.3V_{DD}$	V
V_{IH}	High-level input voltage	5T and 5Tf I/O	$0.7V_{DD}$	-	-	
V_{hys}	Schmidt trigger hysteresis	STD, STDA and 5T, 5Tf I/O	$10\%V_{DD}$	-	-	mV
		Boot0 pin	0.1	-	-	
I_{lkg}	Input leakage current	STDA in digital mode, $V_{DDIOx} \le V_{IN} \le V_{DDA}$	-	-	±1	μA
		5T and 5Tf I/O, $V_{DDIOx} \le V_{IN} \le 5V$	-	-	3	
R_{PU}	Weak pull-up equivalent resistance	Except PA10 and PB12, $V_{IN}=V_{SS}$	30	40	50	kΩ
		PA10 and PB12	7	10	14	
R_{PD}	Weak pull-down equivalent resistance	Except PA10 and PB12, $V_{IN}=V_{DD}$	30	40	50	
		PA10 and PB12	7	10	14	
C_{IO}	I/O pin capacitance	-	-	5	-	pF

Note: (1) The data are obtained from a comprehensive evaluation and are not tested in production.

Table 51 AC Characteristics (T_A=-40℃-105℃)(1)

SPEED[1:0]	Symbol	Parameter	Conditions	Min	Max	Unit
00	$f_{max(IO)out}$	Maximum frequency	CL=50pF,V_{DD}＞2.7V	-	4	MHz
			CL=50pF,V_{DD}＞1.8V	-	2	
			CL=10pF,V_{DD}＞2.7V	-	8	
			CL=10pF,V_{DD}＞1.8V	-	4	

SPEED[1:0]	Symbol	Parameter	Conditions	Min	Max	Unit
	$t_{f(IO)out}/t_{r(IO)out}$	Fall time of output from high to low level and rise time of output from low to high level	C_L=50 pF,V_{DD}=1.8 V-3.6V	-	100	ns
01	$f_{max(IO)out}$	Maximum frequency	CL=50pF,V_{DD}＞2.7V	-	25	MHz
			CL=50pF,V_{DD}＞1.8V	-	12.5	
			CL=10pF,V_{DD}＞2.7V	-	50	
			CL=10pF,V_{DD}＞1.8V	-	20	
	$t_{f(IO)out}/t_{r(IO)out}$	Fall time of output from high to low level and rise time of output from low to high level	CL=30pF,V_{DD}＞2.7V	-	10	ns
			CL=30pF,V_{DD}＞1.8V	-	20	
			CL=10pF,V_{DD}＞2.7V	-	6	
			CL=10pF,V_{DD}＞1.8V	-	10	
10	$f_{max(IO)out}$	Maximum frequency	CL=30pF,V_{DD}＞2.7V	-	50	MHz
			CL=30pF,V_{DD}＞1.8V	-	25	
			CL=10pF,V_{DD}＞2.7V	-	100	
			CL=10pF,V_{DD}＞1.8V	-	50	
	$t_{f(IO)out}/t_{r(IO)out}$	Fall time of output from high to low level and rise time of output from low to high level	CL=30pF,V_{DD}＞2.7V	-	6	ns
			CL=30pF,V_{DD}＞1.8V	-	10	
			CL=10pF,V_{DD}＞2.7V	-	4	
			CL=10pF,V_{DD}＞1.8V	-	6	
11	$f_{max(IO)out}$	Maximum frequency	CL=30pF,V_{DD}＞2.7V	-	100	MHz
			CL=30pF,V_{DD}＞1.8V	-	50	
			CL=10pF,V_{DD}＞2.7V	-	180	
			CL=10pF,V_{DD}＞1.8V	-	100	
	$t_{f(IO)out}/t_{r(IO)out}$	Fall time of output from high to low level and rise time of output from low to high level	CL=30pF,V_{DD}＞2.7V	-	4	ns
			CL=30pF,V_{DD}＞1.8V	-	6	
			CL=10pF,V_{DD}＞2.7V	-	2.5	
			CL=10pF,V_{DD}＞1.8V	-	4	
-	$t_{EINTIpw}$	Pulse width of external signal detected by EINT controller	-	10	-	

Note: (1) The data are obtained from a comprehensive evaluation and are not tested in production.

Figure 12 I/O AC Characteristics Definition

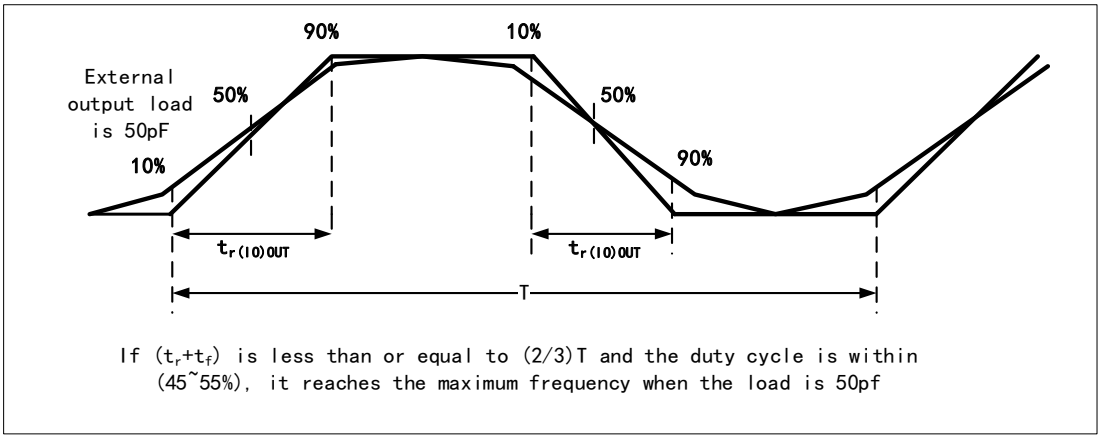


Table 52 Output Drive Voltage Characteristics (T_A=-40℃-105℃)(1)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	I/O pin outputs low voltage	CMOS port, $\|I_{IO}\|$=8mA, 2.7V<V_{DD}<3.6V	-	0.4	V
V_{OH}	I/O pin outputs high voltage		V_{DD}-0.4	-	
V_{OL}	I/O pin outputs low voltage	TTL port, $\|I_{IO}\|$=8mA, 2.7V<V_{DD}<3.6V	-	0.4	
V_{OH}	I/O pin outputs high voltage		2.4	-	
V_{OL}	I/O pin outputs low voltage	$\|I_{IO}\|$=20mA, 2.7V<V_{DD}<3.6V	-	1.3	V
V_{OH}	I/O pin outputs high voltage		V_{DD}-1.3	-	
V_{OL}	I/O pin outputs low voltage	$\|I_{IO}\|$=6mA, 2.7V<V_{DD}<3.6V	-	0.4	
V_{OH}	I/O pin outputs high voltage		V_{DD}-0.4	-	

Note: (1) The data are obtained from a comprehensive evaluation and are not tested in production.

5.11 NRST pin characteristics

The NRST pin input drive adopts CMOS process, which is connected with a permanent pull-up resistor RPU.

Table 53 NRST Pin Characteristics (T_A=-40-105℃, V_{DD}=2-3.6V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST low-level input voltage	TTL port, 2.7V≤V_{DD}≤3.6V	-	-	0.8	V
$V_{IH(NRST)}$	NRST high-level input voltage		2	-	-	
$V_{IL(NRST)}$	NRST low-level input voltage	CMOS port, 1.8V≤V_{DD}≤3.6V	-	-	0.3V_{DD}	
$V_{IH(NRST)}$	NRST high-level input voltage		0.7V_{DD}	-	-	
$V_{hys(NRST)}$	NRST Schmidt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistance	V_{IN}=V_{SS}	30	40	50	kΩ
$V_{F(NRST)}$	NRST input filter pulse	-	-	-	100	ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{NF(NRST)}$	NRST input unfiltered pulse	V_{DD}＞2.7V	300	-	-	
T_{NRST_OUT}	Generated reset pulse duration	Reset internal source	20	-	-	μs

5.12 Communication peripherals

5.12.1 I2C peripheral characteristics

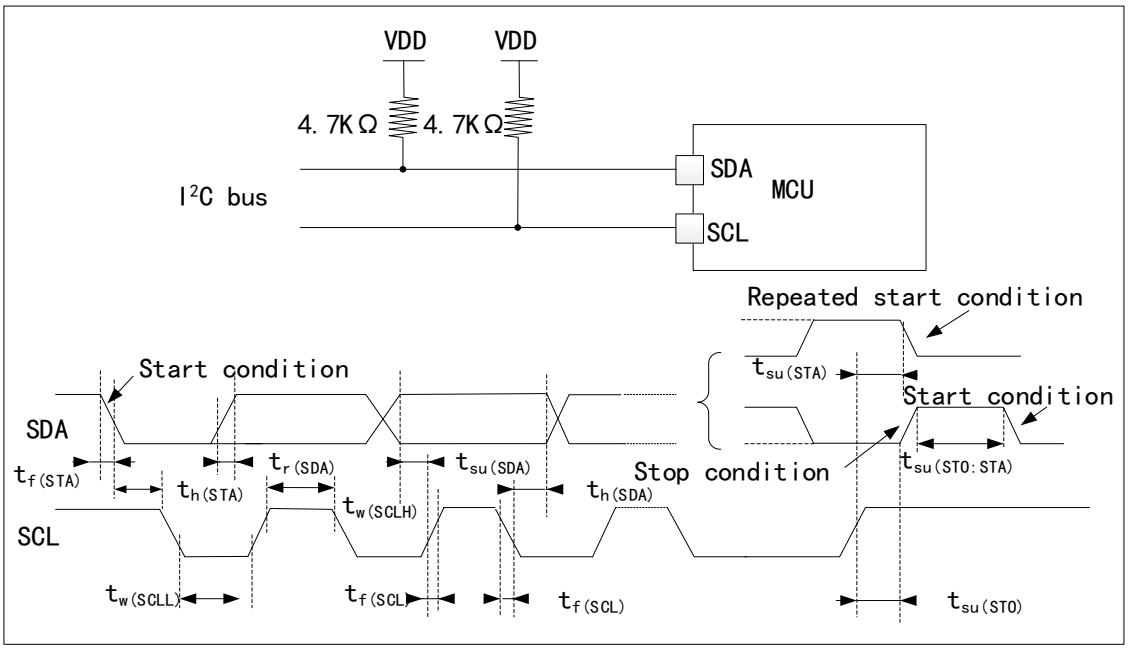
To achieve maximum frequency of I2C in standard mode, f_{PCLK1} must be greater than 2MHz. To achieve maximum frequency of I2C in fast mode, f_{PCLK1} must be greater than 4MHz.

Table 54 I2C Interface Characteristics (T_A=-40℃-105℃, V_{DD}=3.3V)(1)

Symbol	Parameter	Standard I2C		Fast I2C		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	μs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0	-	0	900	
$t_{r(SDA)}/t_{r(SCL)}$	SDA and SCL rise time	-	1000	20+0.1C_b	300	
$t_{f(SDA)}/t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	μs
$t_{su(STA)}$	Setup time of repeated start condition	4.7	-	0.6	-	
$t_{su(STO)}$	Setup time of stop condition	4.0	-	0.6	-	
$t_{w(STO:STA)}$	Time from stop condition to start condition (the bus is idle)	4.7	-	1.3	-	
C_b	Capacitive load of each bus	-	400	-	400	pF

Note: (1) The data are obtained from a comprehensive evaluation and are not tested in production.

Figure 13 Bus AC Waveform and Measurement Circuit



Note: The measuring points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

5.12.2 SPI peripheral characteristics

Table 55 SPI Characteristics (T_A=-40℃-105℃, V_{DD}=3.3V)(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK}	SPI clock frequency	Master mode, SPI1, 2.7V<V_{DD}<3.6V	-	60	MHz
		Slave mode, SPI1, 2.7V<V_{DD}<3.6V	-	60	
$1/t_{c(SCK)}$		Master mode, SPI1/2/3, 1.7V<V_{DD}<3.6V	-	30	
		Slave mode, SPI1/2/3, 1.7V<V_{DD}<3.6V	-	30	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Load capacitance: C=15pF	-	6	ns
$t_{su(NSS)}$	NSS setup time	Slave mode	$4T_{PCLK}$	-	
$t_{h(NSS)}$	NSS hold time	Slave mode	$2T_{PCLK}$ + 10	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode, f_{PCLK}=36MHz, Prescaler factor=4	$T_{PCLK}/2-2$	$T_{PCLK}/2+1$	
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master mode	4	-	
		Slave mode	5	-	
$t_{h(MI)}$ $t_{h(SI)}$	Data input hold time	Master mode	4	-	
		Slave mode	5	-	

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{a(SO)}$	Data output access time	Slave mode, f_{PCLK}=20MHz	0	$3T_{PCLK}$	
$t_{dis(SO)}$	Disable time of data output	Slave mode	0	18	
$t_{v(SO)}$	Effective time of data output	Slave mode (after enabling the edge)	-	22.5	
$t_{v(MO)}$	Effective time of data output	Master mode (after enabling the edge)	-	6.97	
$t_{h(SO)}$	Data output hold time	Slave mode (after enabling the edge)	11.5	-	
$t_{h(MO)}$		Master mode (after enabling the edge)	1	-	
$DuCy_{(SCK)}$	SPI clock frequency duty cycle	Slave mode	25	75	%

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

Figure 14 SPI Timing Diagram - Slave Mode and CPHA=0

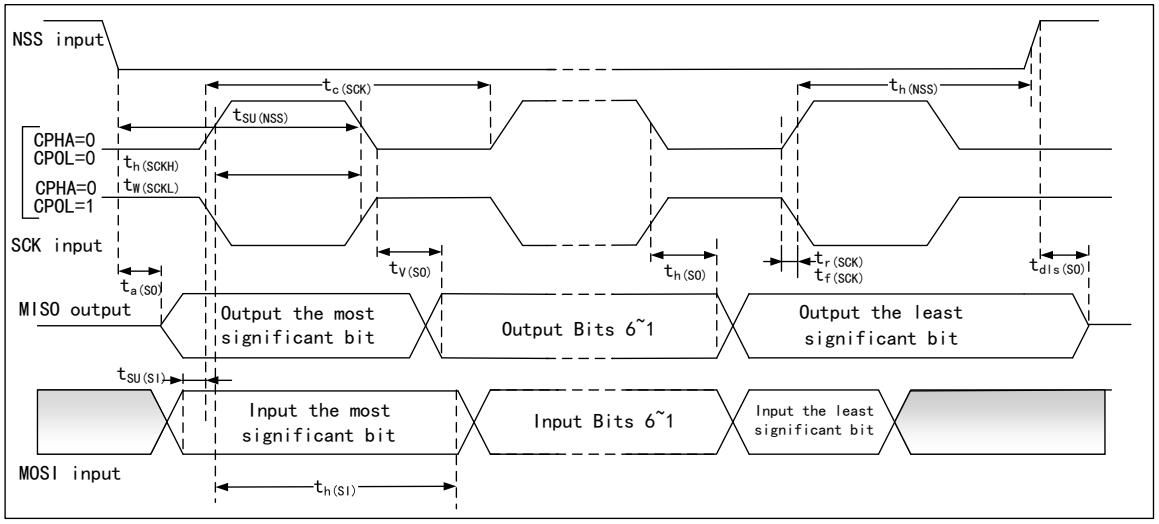
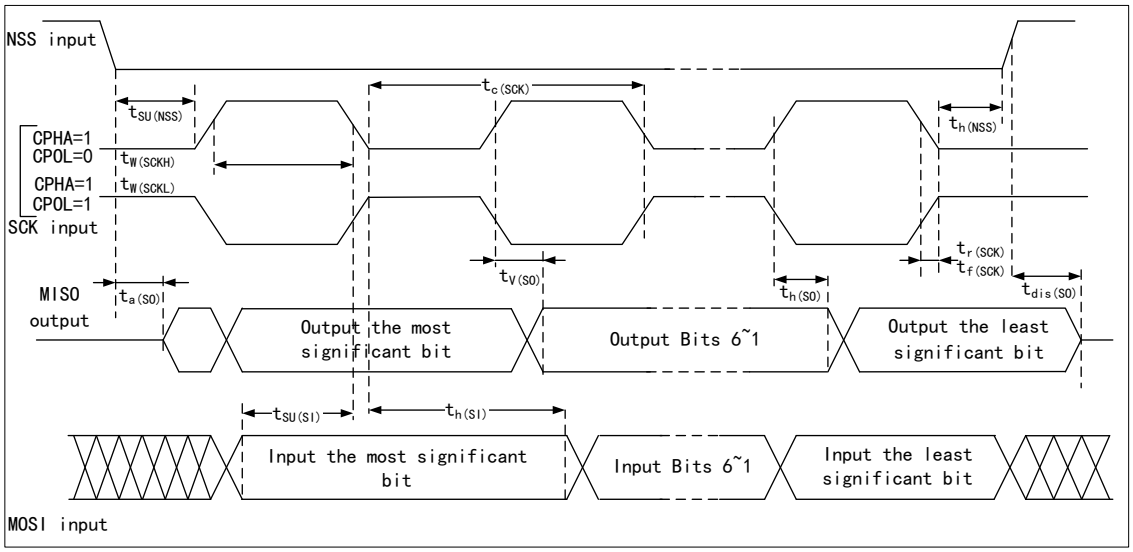
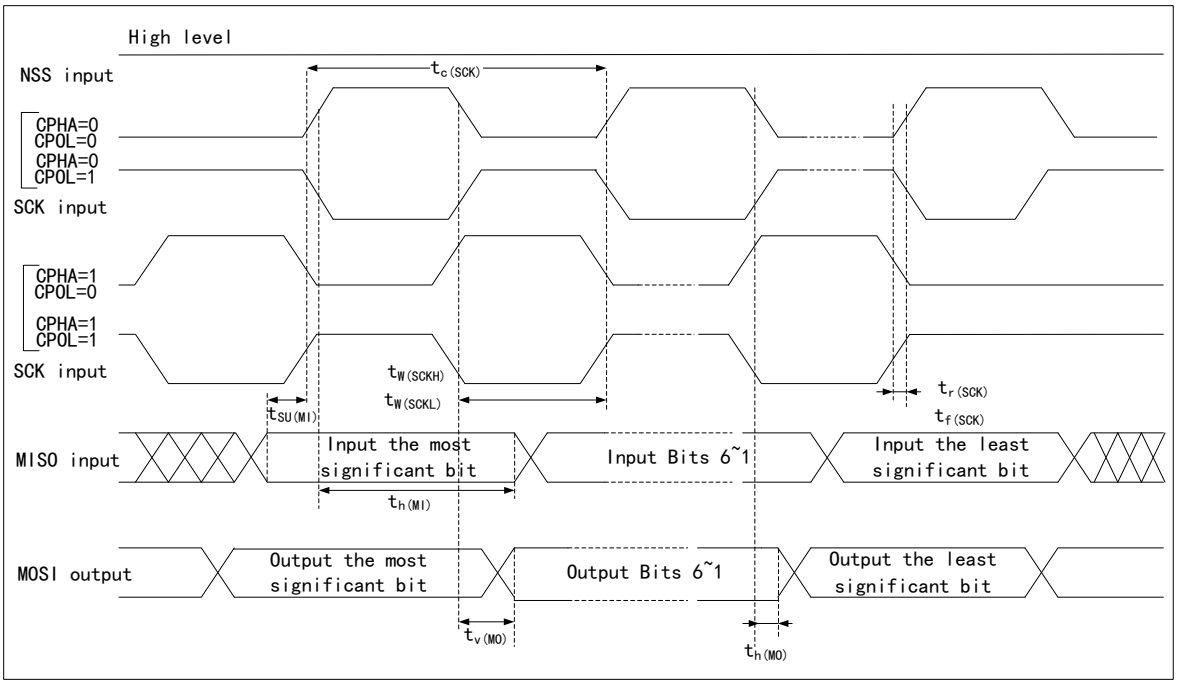


Figure 15 SPI Timing Diagram - Slave Mode and CPHA=1



Note: The measuring points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 16 SPI Timing Diagram - Master Mode



Note: The measuring points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

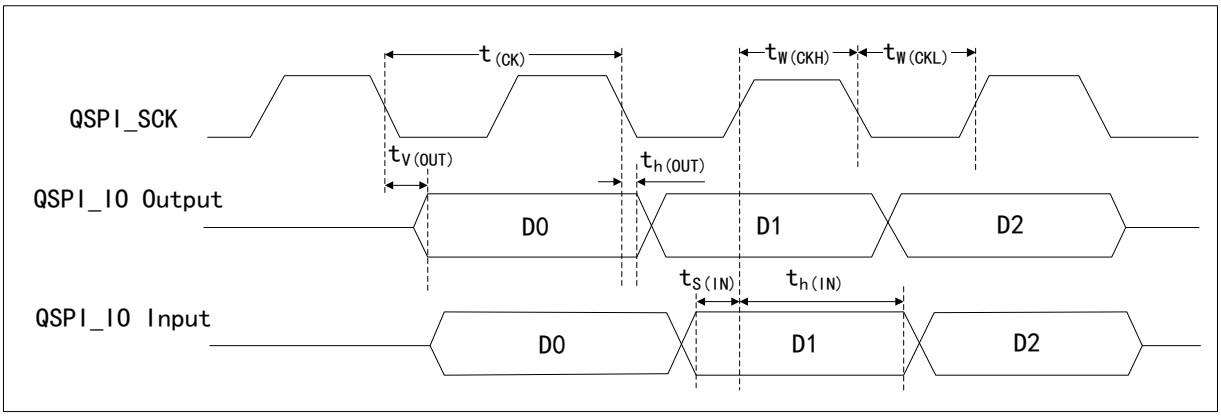
5.12.3 QSPI peripheral characteristics

Table 56 QSPI Peripheral Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{(CK)}$	QSPI clock frequency	-	-	-	120	MHz

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(CKH)}$	QSPI clock high and low time	-	($t_{(CK)}$ / 2) - 2	-	$t_{(CK)}$ / 2	ns
$t_{w(CKL)}$		-	$t_{(CK)}$ / 2	-	$t_{(CK)/2)}$ + 2	
$t_{s(IN)}$	Data input setup time	-	2	-	-	
$t_{h(IN)}$	Data input hold time	-	4.5	-	-	
$t_{v(OUT)}$	Data output valid time	-	-	1.5	3	
$t_{h(OUT)}$	Data output hold time	-	0	-	-	

Figure 17 QSPI Timing Diagram



5.13 Analog peripherals

5.13.1 ADC

Test parameter descriptions:

- Sampling rate: the number of times the ADC converts analog signals to digital signals per second.
- Sample rate=ADC clock / (sampling cycle count + conversion cycle count)

5.13.1.1 12-bit ADC characteristics

Table 57 12-bit ADC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply voltage	-	1.8	-	3.6	V
I_{DDA}	ADC power consumption	-	-	2.0	2.8	mA
f_{ADC}	ADC frequency	V_{DDA}=1.8-2.6V	0.6	15	18	MHz
		V_{DDA}=2.6-3.6V	0.6	20	40	
		V_{DDA}=3.0-3.6V	0.6	30	60	
C_{ADC}	Internal sampling and holding capacitance	-	-	4	-	pF
R_{ADC}	Sampling resistor	-	-	-	6000	Ω

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_S	Sampling time	f_{ADC}=60MHz	0.05	-	8	μs
		-	3	-	480	$1/f_{ADC}$
T_{CONV}	Total conversion time (including sampling time)	f_{ADC}=60MHz 12-bit resolution	0.25	-	8.2	μs
		f_{ADC}=60MHz 10-bit resolution	0.217	-	8.17	μs
		f_{ADC}=60MHz 8-bit resolution	0.18	-	8.13	μs
		f_{ADC}=60MHz 6-bit resolution	0.15	-	8.1	μs
F_S	Sampling rate	f_{ADC}=60MHz 12-bit resolution	0.12	-	4	MSPS
		f_{ADC}=60MHz 10-bit resolution	0.122	-	4.6	
		f_{ADC}=60MHz 8-bit resolution	0.123	-	5.45	
		f_{ADC}=60MHz 6-bit resolution	0.124	-	6.67	
I_{Vref}	In conversion mode, ADC Vref DC power consumption	-	-	150	250	μA
V_{AIN}	ADC analog input	-	0	-	V_{DDA}	V
V_{REFP}	Positive reference voltage	-	1.8	-	V_{DDA}	V
V_{REFN}	Negative reference voltage	-	-	V_{SSA}	-	V
t_{SU}	Startup time (Time from ADC enable to the start of conversion flag set, with default frequency 16MHz)	-	-	2	3	μs

Table 58 12-bit ADC Accuracy(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
E_T	Total error	f_{PCLK}=120MHz, f_{ADC}=60MHz, V_{DDA}=2.6V~3.6V, T_A=-40℃~105℃	±2	±5	LSB
E_O	Offset error		±1.5	±2.5	
E_G	Gain error		±1.5	±3	
E_D	Differential linear error		±1	±2	
E_L	Integral linear error		±1.5	±3	

Note: (1) The data are obtained from a comprehensive evaluation and are not tested in production.

Table 59 ADC Dynamic Accuracy

ADC Dynamic Accuracy	Conditions	Min	Typ	Max	Unit
ENOB (Effective Number of Bits)	Temperature=25℃	10.5	-	-	bit
SNDR (Signal-to-Noise and Distortion Ratio)	Condition 1: V_{DDA}=V_{REFP}=3.3V	-	67.3	-	DB
SNR (Signal-to-Noise Ratio)	f_{ADC}=30MHz, 40MHz, 60MHz	-	67.7	-	
THD (Total Harmonic Distortion)	Input Frequency=110kHz Condition 2: V_{DDA}=V_{REFP}=2.6 V f_{ADC}=30MHz, 40MHz Input Frequency=50kHz	-	-75	-	

5.13.1.2 Temperature sensor characteristics

Table 60 Temperature Sensor Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	Linearity of V_{TS} relative to temperature (T_A = -40~85°C)	-	±1	±2	°C
	Linearity of V_{TS} relative to temperature (T_A = -40~105°C)	-	-	±3	
Slope(1)	Average Slope (V_{DD}=3.3V, T_A=-40~85°C)	2.34	2.47	2.6	mV/ºC
V_{25}	Voltage at 25°C (V_{DD}=2.0-3.6V)	0.7	0.76	0.82	V
T_{S_temp}(2)	ADC sampling time during temperature measurement	10	-	-	μs

Note:

(1) The data are obtained from a comprehensive evaluation and are not tested in production.

(2) The shortest sampling time can be determined by the application program through multiple iterations.

5.13.1.3 Built-in Reference Voltage Characteristics Test

Table 61 Built-in Reference Voltage Characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Built-in Reference Voltage	-40℃ < T_A < +105℃	1.19	1.20	1.20	V
$T_{S\_vrefint}$	Sampling time of ADC when reading internal reference voltage	-	10	-	-	μs
V_{RERINT}	Built-in reference voltage extends to temperature range	V_{DD}=3V	-	3	5	mV
T_{coeff}	Temperature coefficient	-	-	30	50	ppm/℃

Note: (1) The data are obtained from a comprehensive evaluation and are not tested in production.

5.13.2 DAC

Table 62 DAC Characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog power supply voltage	-	1.8	-	3.6	V

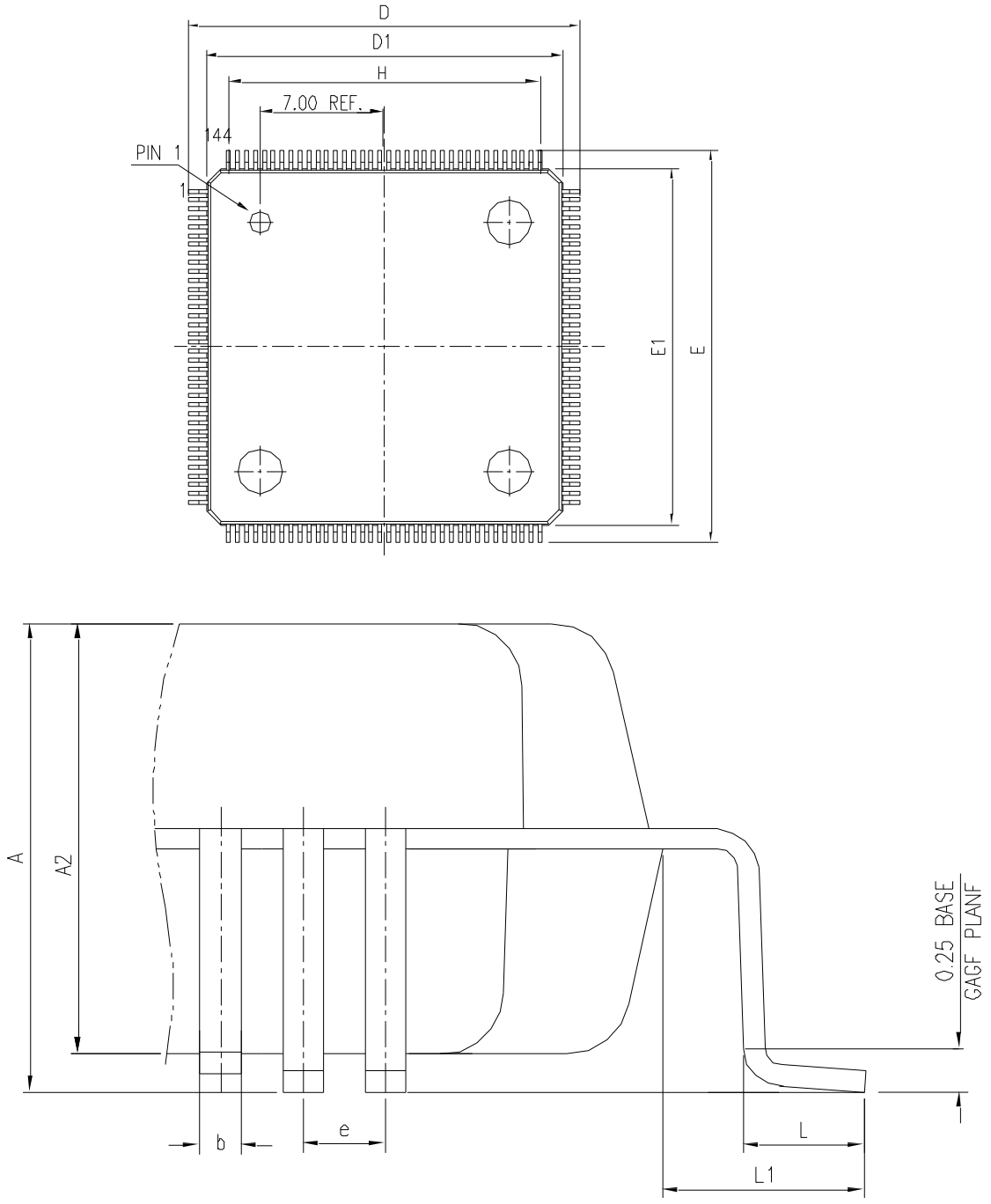
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{LOAD}	Resistive load	The buffer is turned on	5	-	-	kΩ
R_O	Output impedance	The resistive load between DAC_OUT and V_{SS} is 1.5MΩ with buffer off	-	-	15	
C_{LOAD}	Capacitive load	Maximum capacitive load at DAC_OUT pin with buffer on	-	-	50	pF
DAC_OUT Min	Low DAC_OUT voltage with buffer	Maximum output offset of the DAC, corresponding to a 12-bit input code (0x0E0) at V_{REF+} = 3.6V (0xF1C), and at V_{REF+} = 1.8V with codes (0x1C7) and (0xE38).	0.3	-	-	V
DAC_OUT Max	Higher DAC_OUT voltage with buffer		-	-	V_{DDA}-0.3	
DAC_OUT Min	Low DAC_OUT voltage without buffer	Maximum output offset of DAC	-	0.5	-	mV
DAC_OUT Max	Higher DAC_OUT voltage without buffer		-	-	V_{REF+}-1LSB	V
DNL	Differential non-linear error	Configured with 12-bit DAC	-	-	±2	LSB
INL	Integral non-linear error	Configured with 12-bit DAC	-	-	±4	LSB
Offset	Offset error	V_{REF+}=3.6V, configuring 12-bit DAC	-	-	±12	LSB
Gain Error	Gain error	Configured with 12-bit DAC	-	-	±0.5	%

Note: (1) The data are obtained from a comprehensive evaluation and are not tested in production.

6 Package Information

6.1 LQFP144 package information

Figure 18 LQFP144 Package Diagram



（1） The figure is not drawn to scale.

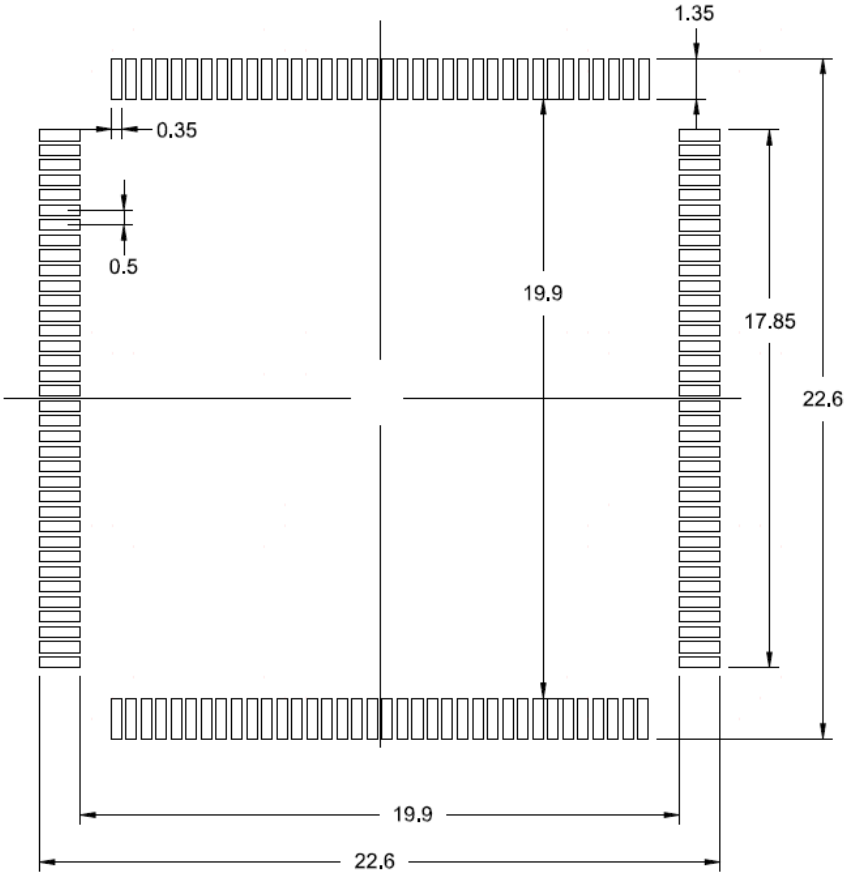
（2） All pins should be soldered to the PCB.

Table 63 LQFP144 Package Data

S/N	SYM	DIMENSIONS	REMARKS
1	A	MAX. 1.600	OVERALL HEIGHT
2	A2	1.400±0.050	PKG THICKNESS
3	D	22.000±0.200	LEAD TIP TO TIP
4	D1	20.000±0.100	PKG LENGTH
5	E	22.000±0.200	LEAD TIP TO TIP
6	E1	20.000±0.100	PKG WIDTH
7	L	0.600±0.150	FOOT LENGTH
8	L1	1.000 REF	LEAD LENGTH
9	e	0.500 BASE	LEAD PITCH
10	H(REF)	(17.50)	CUM LEAD PITCH
11	b	0.22±0.050	LEAD WIDTH

Note: Dimensions are marked in millimeters.

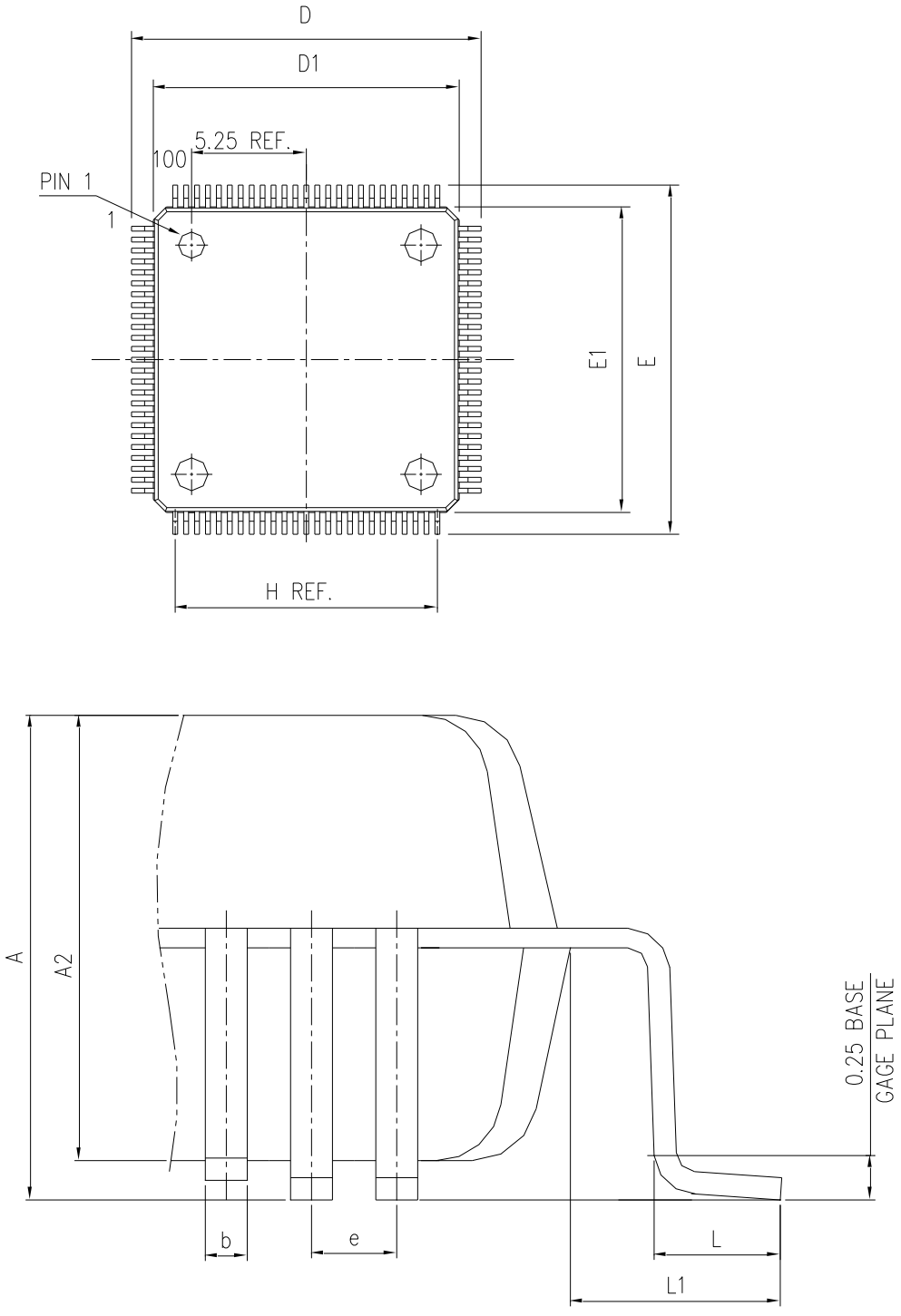
Figure 19 LQFP144 Layout Recommendations



Note: Dimensions are marked in millimeters.

6.2 LQFP100 package information

Figure 20 LQFP100 Package Diagram



（1） The figure is not drawn to scale.

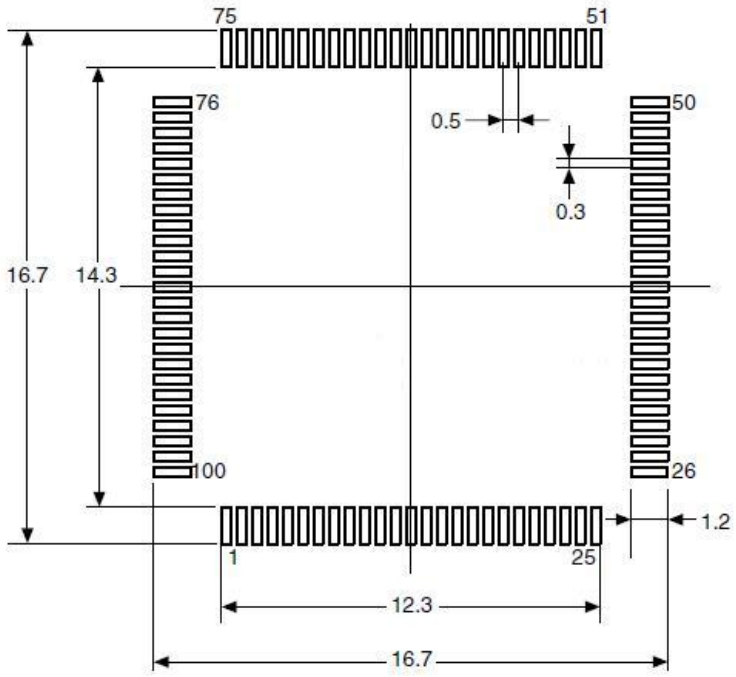
（2） All pins should be soldered to the PCB.

Table 64 LQFP100 Package Data

DIMENSION LIST（FOOTPRINT: 2.00）			
S/N	**SYM**	**DIMENSIONS**	**REMARKS**
1	A	MAX. 1.600	OVERALL HEIGHT
2	A2	1.400±0.050	PKG THICKNESS
3	D	16.000±0.200	LEAD TIP TO TIP
4	D1	14.000±0.100	PKG LENGTH
5	E	16.000±0.200	LEAD TIP TO TIP
6	E1	14.000±0.100	PKG WIDTH
7	L	0.600±0.150	FOOT LENGTH
8	L1	1.000 REF	LEAD LENGTH
9	e	0.500 BASE	LEAD PITCH
10	H（REF）	（12.00）	CUM LEAD PITCH
11	b	0.22±0.050	LEAD WIDTH

Note: Dimensions are marked in millimeters.

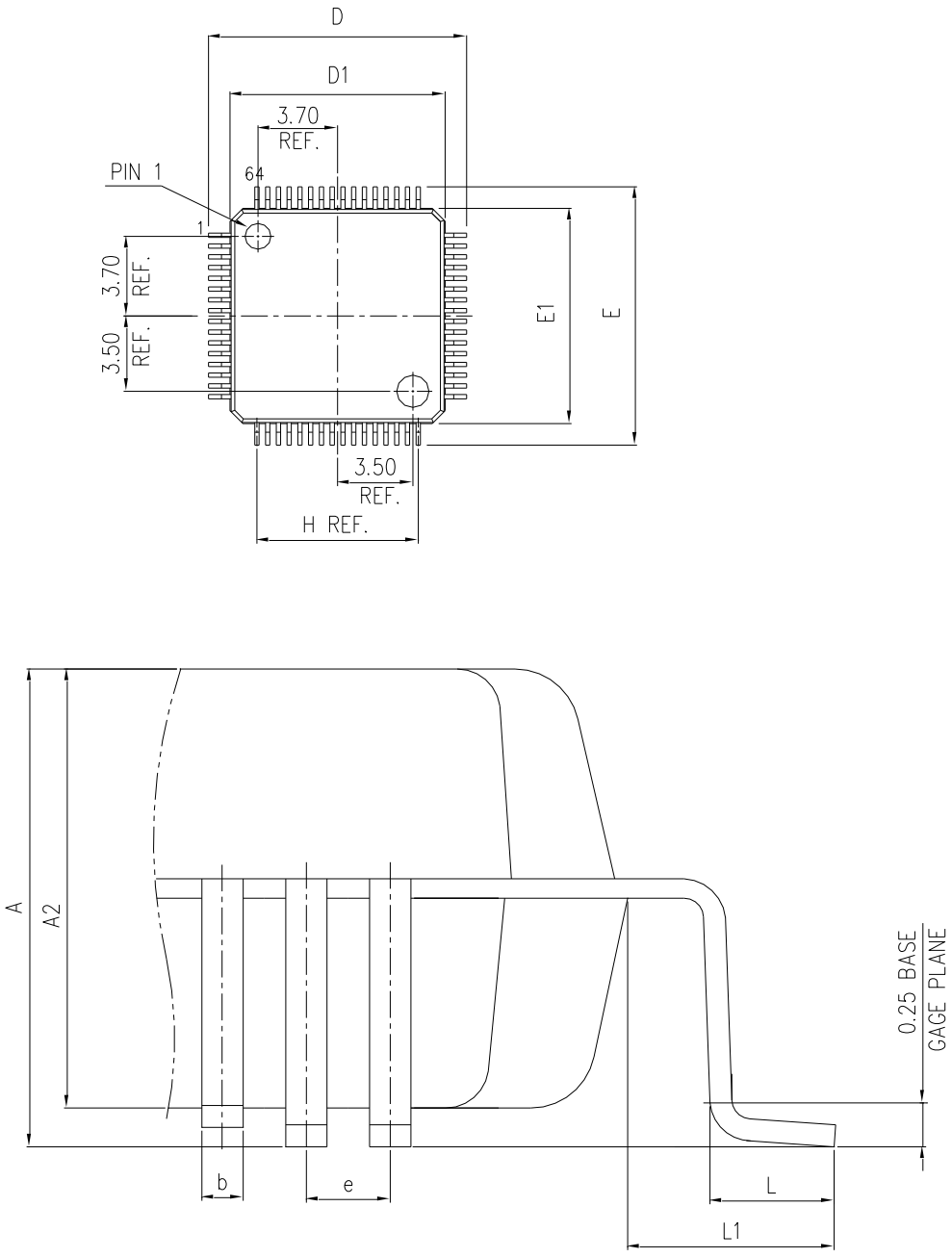
Figure 21 LQFP100 Welding Layout Recommendations



Note: Dimensions are marked in millimeters.

6.3 LQFP64 package information

Figure 22 LQFP64 Package Diagram



（1） The figure is not drawn to scale.

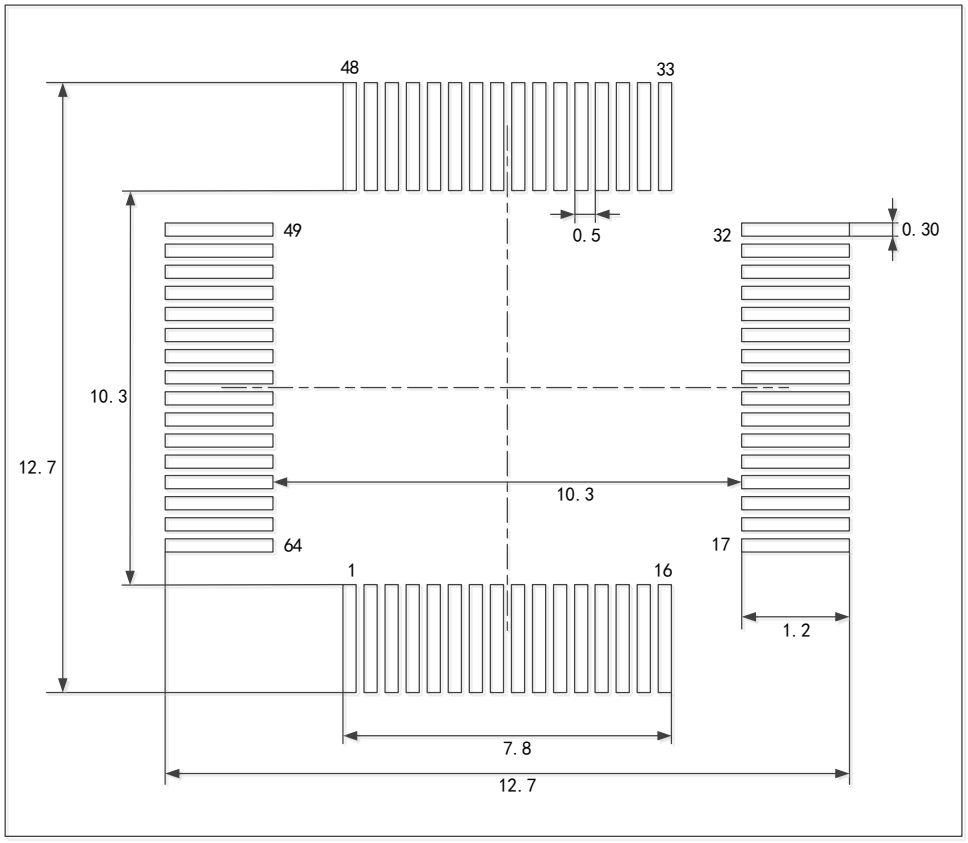
（2） All pins should be soldered to the PCB.

Table 65 LQFP64 Package Data

S/N	SYM	DIMENSIONS	REMARKS
1	A	MAX.1.600	OVERALL HEIGHT
2	A2	1.400±0.050	PKG THICKNESS
3	D	12.000±0.200	LEAD TIP TO TIP
4	D1	10.000±0.100	PKG LENGTH
5	E	12.000±0.200	LEAD TIP TO TIP
6	E1	10.000±0.100	PKG WIDTH
7	L	0.600±0.150	FOOT LENGTH
8	L1	1.000REF.	LEAD LENGTH
9	e	0.500BASE	LEAD PITCH
10	H(REF)	(7.500)	CUM LEAD PITCH
11	b	0.220±0.050	LEAD WIDTH

Note: Dimensions are marked in millimeters.

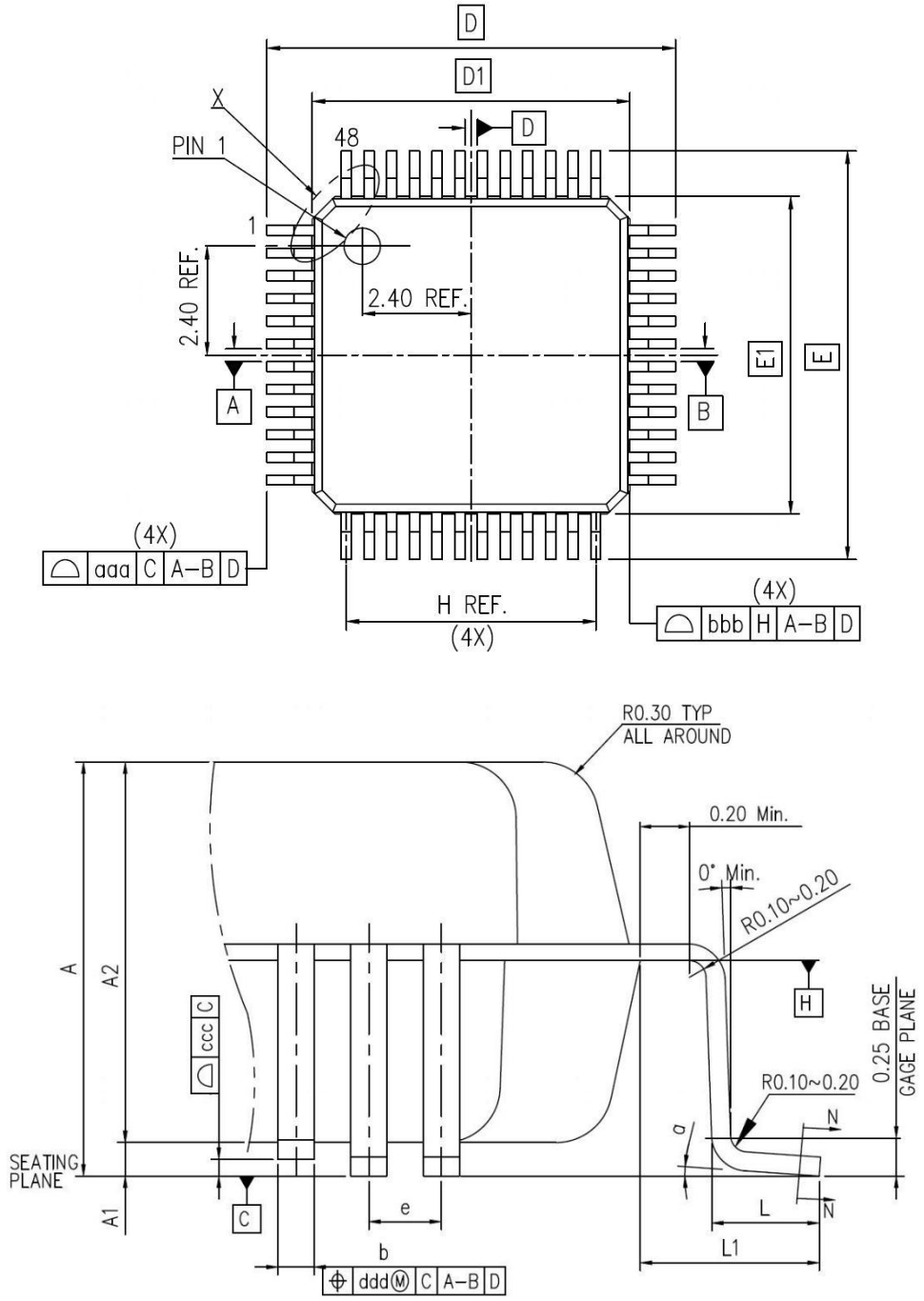
Figure 23 LQFP64 Welding Layout Recommendations



Note: Dimensions are marked in millimeters.

6.4 LQFP48 package information

Figure 24 LQFP48 Package Diagram



（1） The figure is not drawn to scale.

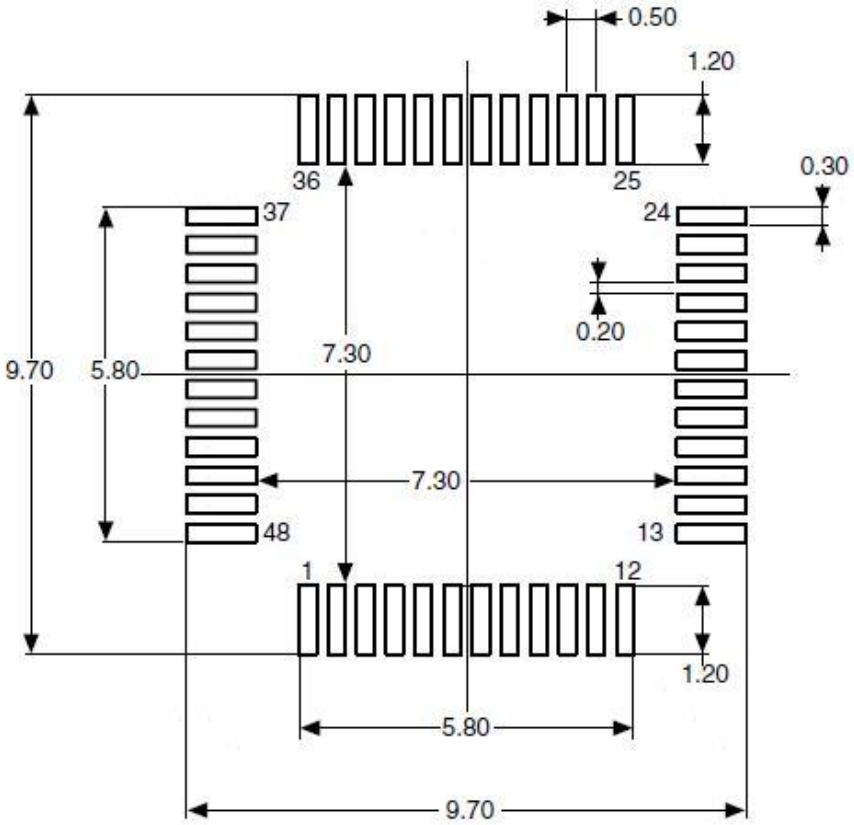
（2） All pins should be soldered to the PCB.

Table 66 LQFP48 Package Data

DIMENSION LIST (FOOTPRINT: 2.00)			
S/N	SYM	DIMENSIONS	REMARKS
1	A	MAX. 1.60	OVERALL HEIGHT
2	A1	0.1±0.05	STANDOFF
3	A2	1.40±0.05	PKG THICKNESS
4	D	9.00±0.20	LEAD TIP TO TIP
5	D1	7.00±0.10	PKG LENGTH
6	E	9.00±0.20	LEAD TIP TO TIP
7	E1	7.00±0.10	PKG WIDTH
8	L	0.60±0.15	FOOT LENGTH
9	L1	1.00 REF	LEAD LENGTH
10	T	0.15	LEAD THICKNESS
11	T1	0.127±0.03	LEAD BASE METAL THICKNESS
12	a	0°~7°	FOOT ANGLE
13	b	0.22±0.02	LEAD WIDTH
14	b1	0.20±0.03	LEAD BASE METAL WIDTH
15	e	0.50 BASE	LEAD PITCH
16	H(REF.)	(5.50)	CUM. LEAD PITCH
17	aaa	0.2	PROFILE OF LEAD TIPS
18	bbb	0.2	PROFILE OF MOLD SURFACE
19	ccc	0.08	FOOT COPLANARITY
20	ddd	0.08	FOOT POSITION

Note: Dimensions are marked in millimeters.

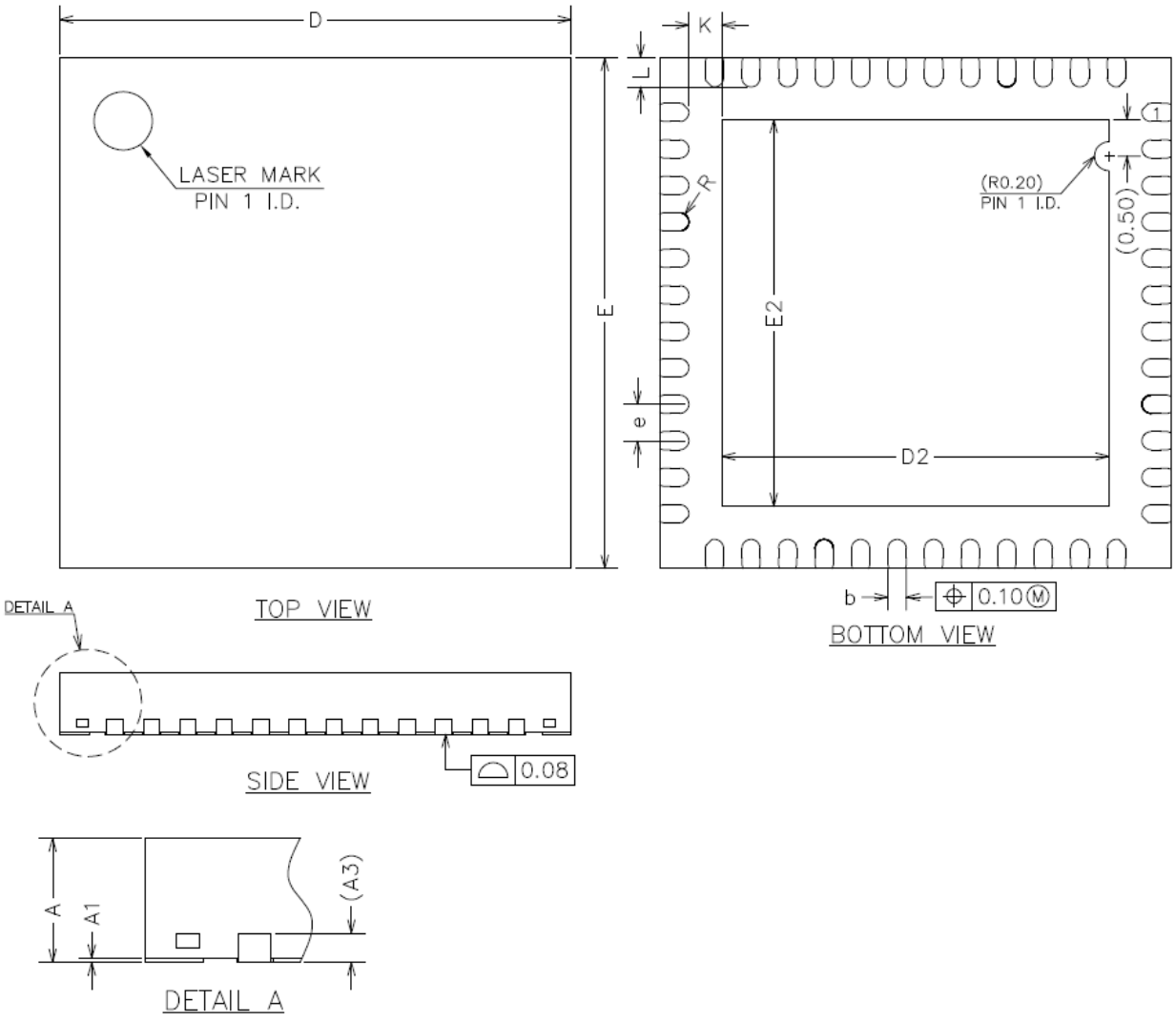
Figure 25 LQFP48 Welding Layout Recommendations



Note: Dimensions are marked in millimeters.

6.5 QFN48 package information

Figure 26 QFN48 Package Diagram



（1） The figure is not drawn to scale.

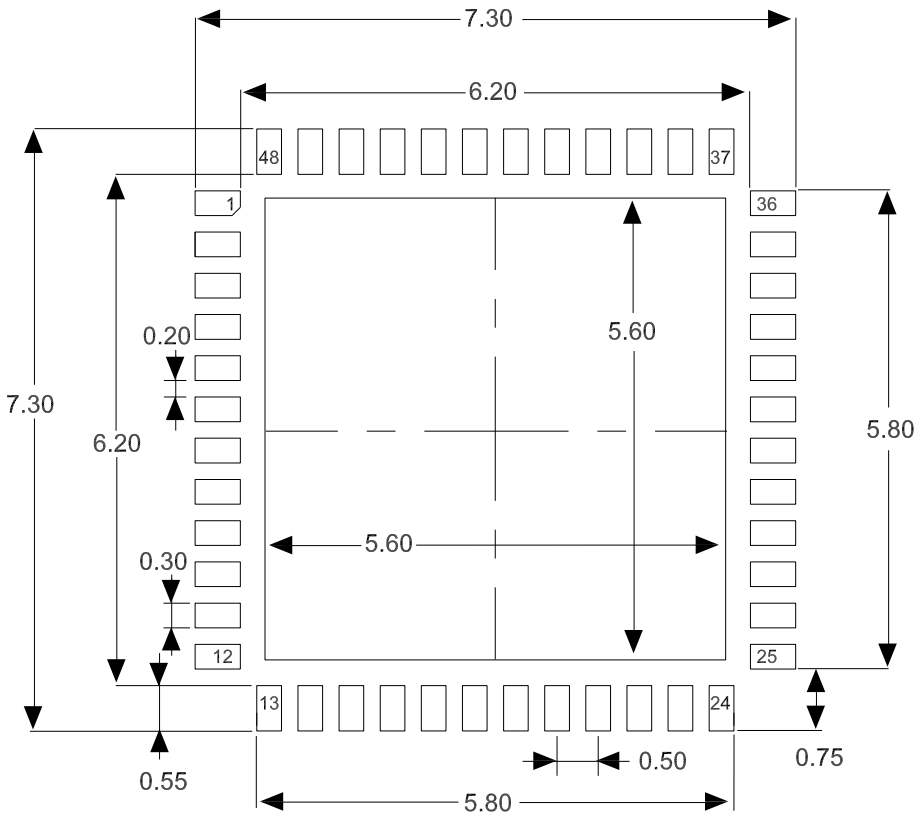
（2） All pins should be soldered to the PCB.

Table 67 QFN48 Package Data

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20REF		
b	0.20	0.25	0.30

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	6.90	7.00	7.10
E	6.90	7.00	7.10
D2	5.20	5.30	5.40
E2	5.20	5.30	5.40
e	0.40	0.50	0.60
K	0.35	0.45	0.55
L	0.30	0.40	0.50
R	0.09	-	-

Figure 27 QFN48 Welding Layout Recommendations



Note: Dimensions are marked in millimeters.

6.6 Package identification

The package identification of LQFP and QFN is listed below:

Figure 28 Package Identification

Table 68 Silkscreen Descriptions

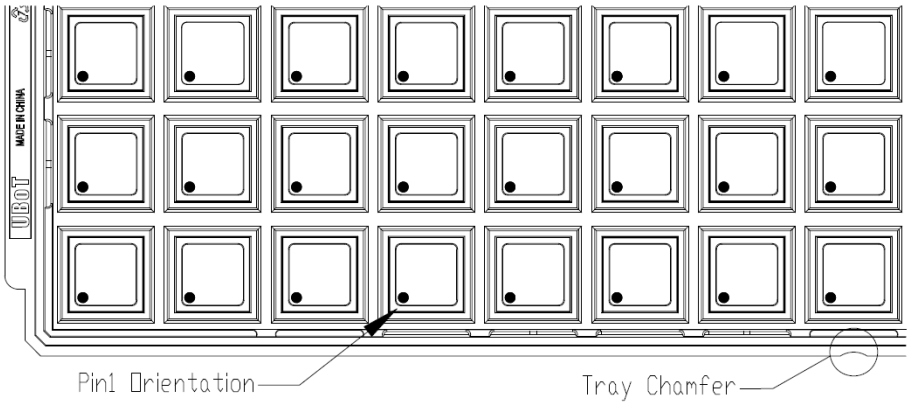
Symbol	Descriptions
Geehy	Company Name
XXXXXXX	Device Family
XXXXXXXX	Product Model
LLLLLLLL	Batch Number
CCCC	Internal Traceable Code
YYWW	Year and Week Number
arm	Arm® Authorized Trademark
●	PIN1 Location

Note: The length of each line may vary and is not fixed.

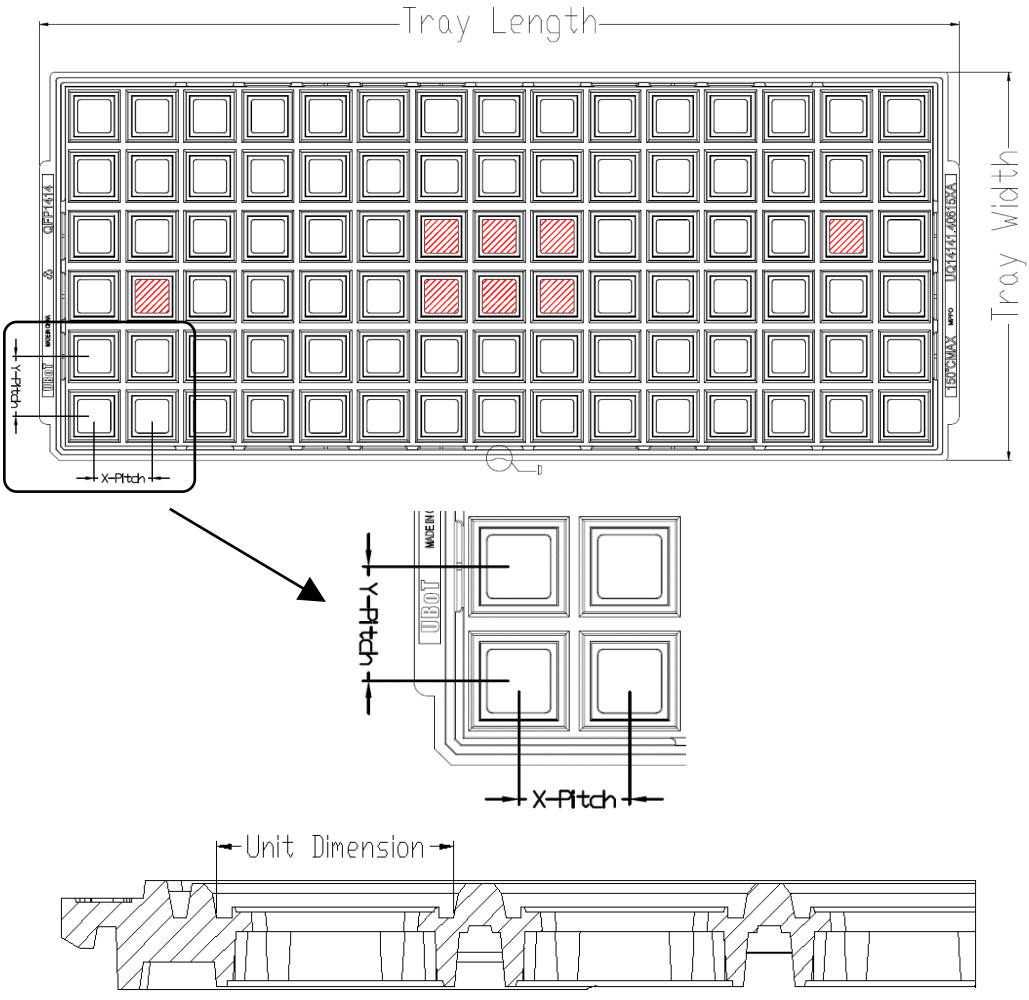
7 Packaging Information

7.1 Tray packaging

Figure 29 Tray Packaging Diagram



Tray Dimensions



All photos are for reference only, and the appearance is subject to the product.

Table 69 Tray Packaging Parameter Specification Table

Device	Package Type	Pins	SPQ	X-Dimension（mm）	Y-Dimension（mm）	X-Pitch（mm）	Y-Pitch（mm）	Tray Length（mm）	Tray Width（mm）
APM32F427ZGT6	LQFP	144	600	22.06	22.06	25.4	25.2	322.6	135.9
APM32F427VGT6	LQFP	100	900	16.6	16.6	20.3	21	322.6	135.9
APM32F427RGT6	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
APM32F427CGT6	LQFP	48	2500	9.7	9.7	12.2	12.6	322.6	135.9
APM32F427CGU6	QFN	48	2600	7.25	7.25	11.8	12.8	322.6	135.9
APM32F427ZGT7	LQFP	144	600	22.06	22.06	25.4	25.2	322.6	135.9
APM32F427VGT7	LQFP	100	900	16.6	16.6	20.3	21	322.6	135.9
APM32F427RGT7	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
APM32F427CGT7	LQFP	48	2500	9.7	9.7	12.2	12.6	322.6	135.9
APM32F427CGU7	QFN	48	2600	7.25	7.25	11.8	12.8	322.6	135.9
APM32F425ZGT6	LQFP	144	600	22.06	22.06	25.4	25.2	322.6	135.9
APM32F425VGT6	LQFP	100	900	16.6	16.6	20.3	21	322.6	135.9
APM32F425RGT6	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
APM32F425CGT6	LQFP	48	2500	9.7	9.7	12.2	12.6	322.6	135.9
APM32F425CGU6	QFN	48	2600	7.25	7.25	11.8	12.8	322.6	135.9
APM32F425ZGT7	LQFP	144	600	22.06	22.06	25.4	25.2	322.6	135.9
APM32F425VGT7	LQFP	100	900	16.6	16.6	20.3	21	322.6	135.9
APM32F425RGT7	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
APM32F425CGT7	LQFP	48	2500	9.7	9.7	12.2	12.6	322.6	135.9
APM32F425CGU7	QFN	48	2600	7.25	7.25	11.8	12.8	322.6	135.9

8 Ordering Information

Table 70 Ordering Information Table

Product Name			
APM32F427ZGT6			
Example	**Definition**	**Naming**	**Description**
APM32	Device Family	APM32	ARM-based 32-bit microcontroller
F	Product Model	F	Basic model
427	Product Subtype	425/427	High performance
Z	Number of Pins	C	48 pins
		R	64 pins
		V	100 pins
		Z	144 pins
G	Flash Memory Size	G	1MB
T	Package Type	T	LQFP
		U	QFN
6	Temperature Range	6	Industrial grade -40℃~85℃
		7	Industrial grade -40℃~105℃
R	Options	XXX	Pre-programmed device code
		R	Tape and reel packaging
		Blank	Tray packaging
		T	Tube packaging

Table 71 Ordering Information Table

Order code	FLASH（KB）	SRAM（KB）	Package	SPQ	Range of temperature
APM32F427ZGT6	1024	448+4	LQFP144	600	Industrial grade -40℃~85℃
APM32F427VGT6	1024	448+4	LQFP100	900	Industrial grade -40℃~85℃
APM32F427RGT6	1024	448+4	LQFP64	1600	Industrial grade -40℃~85℃
APM32F427CGT6	1024	448+4	LQFP48	2500	Industrial grade -40℃~85℃
APM32F427CGU6	1024	448+4	QFN48	2600	Industrial grade -40℃~85℃
APM32F427ZGT7	1024	448+4	LQFP144	600	Industrial grade -40℃~105℃
APM32F427VGT7	1024	448+4	LQFP100	900	Industrial grade -40℃~105℃
APM32F427RGT7	1024	448+4	LQFP64	1600	Industrial grade -40℃~105℃
APM32F427CGT7	1024	448+4	LQFP48	2500	Industrial grade -40℃~105℃
APM32F427CGU7	1024	448+4	QFN48	2600	Industrial grade -40℃~105℃
APM32F425ZGT6	1024	192+4	LQFP144	600	Industrial grade -40℃~85℃
APM32F425VGT6	1024	192+4	LQFP100	900	Industrial grade -40℃~85℃
APM32F425RGT6	1024	192+4	LQFP64	1600	Industrial grade -40℃~85℃

Order code	FLASH（KB）	SRAM（KB）	Package	SPQ	Range of temperature
APM32F425CGT6	1024	192+4	LQFP48	2500	Industrial grade -40℃~85℃
APM32F425CGU6	1024	192+4	QFN48	2600	Industrial grade -40℃~85℃
APM32F425ZGT7	1024	192+4	LQFP144	600	Industrial grade -40℃~105℃
APM32F425VGT7	1024	192+4	LQFP100	900	Industrial grade -40℃~105℃
APM32F425RGT7	1024	192+4	LQFP64	1600	Industrial grade -40℃~105℃
APM32F425CGT7	1024	192+4	LQFP48	2500	Industrial grade -40℃~105℃
APM32F425CGU7	1024	192+4	QFN48	2600	Industrial grade -40℃~105℃

9 Commonly Used Function Module

Table 72 Commonly Used Function Module

Full name	Abbreviations
Reset management unit	RMU
Clock management unit	CMU
Reset and clock management	RCM
External interrupt	EINT
General-purpose IO	GPIO
Multiplexing IO	AFIO
Wake-up controller	WUPT
Buzzer	BUZZER
Independent watchdog timer	IWDT
Window watchdog timer	WWDT
Timer	TMR
CRC controller	CRC
Power management unit	PMU
DMA controller	DMA
Analog-to-digital converter	ADC
Real-time clock	RTC
External memory controller	EMMC
Static memory controller	SMC
Dynamic memory controller	DMC
Controller local area network	CAN
I2C interface	I2C
Serial peripheral interface	SPI
Universal asynchronous transmitter receiver	UART
Universal synchronous and asynchronous transmitter receiver	USART
Flash interface control unit	FMC
Quad serial peripheral interface	QSPI
Random number generator	RNG

10 Version History

Table 73 Document Version History

Date	Version	Change History
July 2025	1.0	New
August 2025	1.1	Modify DAC electrical characteristics data

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8. Scope of Application

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